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The LTC1625 Current Mode DC/DC Controller Eliminates the Sense Resistor

by Christopher B. Umminger

Introduction

Power supply designers have a new tool in their quest for ever higher efficiencies. In the past, when designing a step-down DC/DC converter, one had to choose between the high efficiency of voltage mode control and the many benefits of current mode control. Although voltage mode control offers high efficiency and a simple topology, it is difficult to compensate, has poor rejection of input-voltage transients and does not inherently limit output current under fault conditions, such as an output short circuit. Current mode control overcomes these problems by adding a control loop to regulate the inductor current in addition to the output voltage. Unfortunately, a sense resistor is required to measure this current, which adds cost and complexity while reducing converter efficiency. However, with the new LTC1625 No R_{SENSE} [™] controller, one can enjoy all of the benefits of current mode control without the penalties of using a sense resistor.

The LTC1625 is a step-down DC/DC switching regulator controller that incorporates popular features from the LTC1435 and related parts. It is capable of a wide range of operation with inputs from 3.7V to 36V. Fixed output voltages of 5V and 3.3V can be selected or an external resistive divider can be used to obtain output voltages

from 1.19V up to nearly the full input voltage. The controller provides synchronous drive for N-channel power MOSFETs and retains the advantage of low dropout operation typically associated with P-channel MOSFETs. Burst Mode[™] operation maintains efficiency at low load currents, but can be overridden to assist secondary-winding regulation by forcing continuous operation. In addition to eliminating the sense resistor, the LTC1625 further reduces the external parts count by incorporating the oscillator timing capacitor. The oscillator frequency can be set to 150kHz, 225kHz, or can be injection locked to any frequency between these points.

Current Mode Control without a Sense Resistor

How does one implement current mode control without a current sense resistor? The answer is to make the standard power MOSFET switches do double duty as current sense elements. By measuring the drain-to-source voltage of a MOSFET operating in the triode region, one can use the $R_{DS(ON)}$ of the device as a sense resistance. Although conceptually simple, this is tricky to implement in practice because inductor current information can only be obtained when a MOSFET is turned on. Figure 1

continued on page 3



Issue Highlights

The lead article this month features the new LTC1625 No R_{SENSE} DC/DC controller. The LTC1625 is a step-down DC/DC switching regulator controller that incorporates popular features from the LTC1435 and related parts. The LTC1625 provides all of the benefits of current mode control without the penalties of using a sense resistor. How does one implement current mode control without a current sense resistor? The answer is to make the standard power MOSFET switches do double duty as current sense elements.

Several other new power control products are also introduced in this issue. The LTC1627 is a new addition to a growing family of power management products optimized for Li-Ion batteries. Li-Ion batteries, with their high energy density, are becoming the chemistry of choice for many handheld products. The LTC1627 monolithic, current mode synchronous buck regulator was specifically designed to meet these demands. With its operating supply range of 2.65V to 8.5V, it can operate from one or two Li-Ion batteries as well as 3- to 6-cell NiCd and NiMH battery packs.

LTC1435A is an improved version of the LTC1435 synchronous DC/DC controller. It has all the outstanding features of the LTC1435, with a reduced minimum on-time of 300ns or less, and improved noise immunity at low output voltages. With these improvements, high performance at output voltages down to 1.3V can be achieved with operating frequencies in excess of 250kHz from input supply voltages above 22V.

To accommodate the precise, yet varied voltage requirements of the next generation of microprocessors, LTC introduces the LTC1706-19 VID voltage programmer. This device is a precision, digitally programmable resistive divider that enables an entire family of LTC's DC/DC converters with onboard 1.19V references to produce output voltages from 1.30V to 2.00V in 0.05V steps.

The LT[®]1506 is a 500kHz monolithic buck mode switching regulator, functionally identical to the LT1374 but optimized for lower input voltage applications. Its high 4.5A switch rating makes this device suitable for use as the primary regulator in small to medium power systems.

In the data conversion arena, we debut the LTC1412, a new 12-bit 3Msps ADC that brings new levels of performance and ease of use to high speed ADC applications. By raising the speed of the successive approximation (SAR) method to 3Msps, it eliminates the many drawbacks of pipelined and subranging ADCs in that speed range. It is the first clean, simple to use alternative to pipelined ADCs for applications up to 3Msps.

Also in this issue, we premier several new members of the LTC1068 family of universal switched capacitor filters. Each product contains four matched, low noise, high accuracy 2nd order switched capacitor filter sections. High precision, high performance, quad 2nd order, dual 4th order or single 8th order filters can be designed with an LTC1068 family product.


Rounding out the Design Features section, we have four new Hot Swap[™] controllers. The LTC1640H and LTC1640L provide a simple, flexible solution to -48V hot swapping. The chips allow a board to be safely inserted into or removed from a live backplane with a supply voltage from -10V to -80V. The "H" and "L" parts are intended for use with modules with active high and active low enable inputs, respectively. The LTC1643 is a Hot Swap controller for PC bus application. The LTC1643H is designed for motherboard applications, whereas the LTC1643L is designed for CompactPCI[™] applications where the chip resides on the plug-in board.

CompactPCI is a trademark of the PCI Industrial Computer Manufacturers' Group.

LTC in the News...

The July 13, 1998 issue of *Business Week* included the magazine's annual "Business Week Global 1000" rankings of the top U.S. and international corporations according to market capitalization. Linear Technology made both the U.S. and global lists, coming in at number 373 in the United States and 768 worldwide. The Company also made *Equities* magazine's annual "America's Most Profitable Companies" issue at the end of June, ranking at number 100 among the most profitable public companies traded on the Nasdaq.

On July 21, Linear Technology announced its financial results for fiscal year 1998. Said Robert H. Swanson, President and CEO, "Fiscal 1998 was a good year for Linear Technology as we achieved record levels of sales and earnings." Specifically, the Company reported net sales for the fourth quarter of \$132,011,000 (a 27% increase over net sales for the fourth quarter of the previous year), net income for the quarter of \$49,503,000 (up 32% from the previous fiscal year's fourth quarter). For the year, the Company's net sales were \$484,799,000 (up 28% compared to the previous year), with net income of \$180,902,000 (up 35% versus the prior year). 

The Design Information section includes part one of an article on achieving and measuring settling times for 16-bit DACs and the LTC1650, a new 16-bit bipolar output DAC in the SO-16 package. The Design Ideas section includes a low noise 33V varactor bias supply, a low noise 5V to -5V/200mA DC/DC converter, a crystal oscillator with 50% duty cycle and complementary outputs, a circuit to provide a ground-referenced output voltage that is proportional to a measured current. We conclude with a quintet of New Device Cameos. 

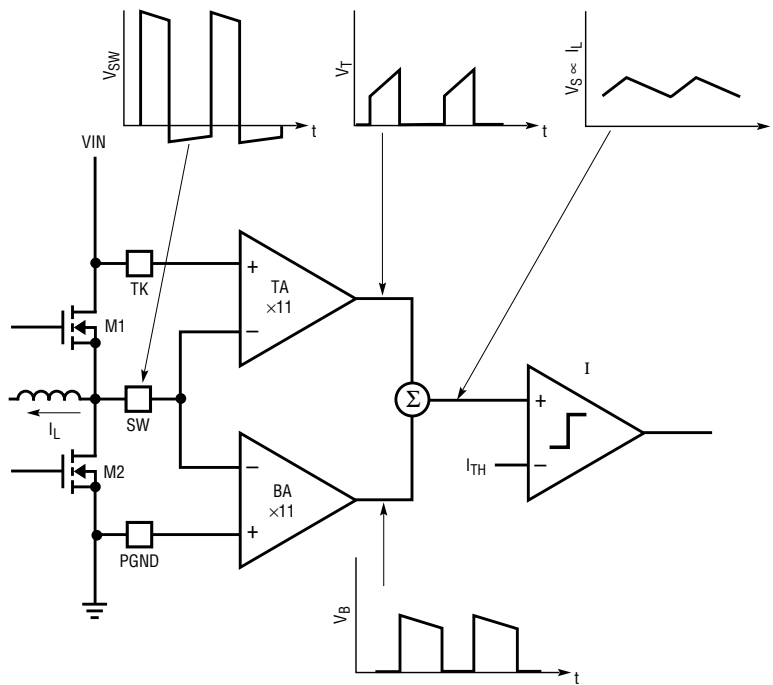


Figure 1. The LTC1625 senses V_{DS} across the power MOSFETs to infer inductor current.

Easing the Layout Challenge

Ensuring that switching transients do not interfere with the control loop is a common difficulty with high output-current power converters. A great deal of effort is often expended in board layout and component placement to subdue coupling effects, such as pulse pairing or grouping. Eliminating the sense resistor and its associated signal lines makes this job easier. In addition, the LTC1625 uses some internal blanking around the switching transitions to further reduce the possibility of jitter or pulse pairing in the control loop. The result is a controller that is relatively immune to these coupling effects and remarkably easy to lay out successfully. On the other hand, the addition of blanking increases the minimum time in which the controller can turn the top MOSFET on and off. This places a limit on the minimum duty cycle but does not unduly restrict the maximum input voltage for a given output voltage. Table 1 shows the many common input and output voltage combinations that the LTC1625 can accommodate.

Additional Features

The LTC1625 controller is designed for synchronous, step-down applications with two N-channel power MOSFETs. Using an N-channel MOSFET for the topside switch is more cost-effective than using a P-channel device, but it requires a floating topside driver. This driver is powered using an external bootstrap capacitor and diode. If the input voltage

LTC1625, continued from page 1

illustrates how this is accomplished in the LTC1625. The drain-to-source voltages of the power MOSFETs are sensed through the TK, SW and PGND pins. Sense amplifiers TA and BA measure and amplify these voltages only when the respective MOSFET is conducting current. The two resulting signals (V_T and V_B) are summed to create a sense voltage ramp (V_S) that is proportional to the inductor current throughout the entire switching cycle. A current comparator (I) uses the sense voltage and a current threshold voltage (I_{TH}) to control the power MOSFETs. Because the LTC1625 fully recovers the inductor current information, it behaves

identically to traditional current mode controllers that use a sense resistor.

An important feature of current mode control is its ability to inherently limit load current simply by restricting the range of the current-threshold voltage. The maximum allowed current is then inversely proportional to the sense resistance. With the LTC1625, the power MOSFET on-resistance determines the maximum output current. An approximate graph of this relationship is shown in Figure 2, along with data points for some popular Siliconix MOSFETs. The on-resistance is typically guaranteed to be below a maximum specified by the manufacturer, but it will vary substantially between lots and over temperature. Thus, a design accommodating the maximum possible on-resistance will have a significantly higher maximum output current when this resistance is lower than normal. To ensure reasonable current levels in case of a fault, such as an output short to ground, the LTC1625 will fold back the current if the output voltage falls significantly.

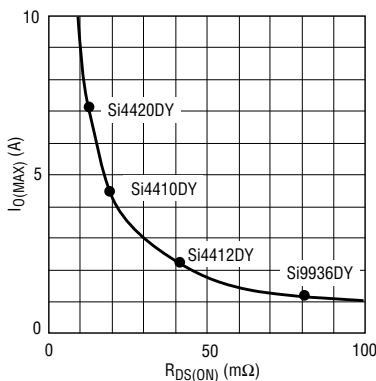


Figure 2. Maximum output current is determined primarily by the on-resistance of the power MOSFETs.

Table 1. Some common input and output voltage combinations available with $f_{OSC} = 150kHz$

V_{OUT} (V)	V_{IN} (V)				
	5	12	18	24	30
1.5	✓	✓			
1.8	✓	✓	✓		
2.5	✓	✓	✓	✓	
3.3	✓	✓	✓	✓	✓
5.0		✓	✓	✓	✓
12.0			✓	✓	✓

drops close to the output voltage, the LTC1625 will begin skipping cycles, leaving the top MOSFET on longer in order to maintain low dropout operation. Once in dropout, the boost capacitor is recharged by turning off the top MOSFET and turning on the bottom MOSFET briefly every tenth cycle. This maintains a duty cycle greater than 99% in dropout.

Another external part was eliminated by incorporating the oscillator timing capacitor into the LTC1625. The controller runs at a nominal 150kHz frequency that can be increased 50% by taking the SYNC pin above 1.2V. Frequency-sensitive applications can synchronize the oscillator by applying a clock signal between 165kHz and 200kHz to this pin.

Providing gate charge to the power MOSFET switches is one of the main sources of efficiency loss in switching regulators. The LTC1625 includes two features to minimize this loss. Normally, both MOSFETs are turned on and off once per oscillator cycle. When the load current drops to near zero, the gate charge required for switching becomes a significant fraction of the total input current. The LTC1625 addresses this problem with Burst Mode operation. As the load current decreases below approximately one fifth of its maximum value, both MOSFETs are turned off for a few cycles while the output capacitors support the load. In this way, gate charge is saved at the expense of fixed frequency operation. For applications that require it, fixed frequency operation can be maintained by tying the FCB pin low to force continuous operation at low load currents. This pin can also be used to adaptively override Burst Mode operation when regulating the output of a secondary winding. Another problem with gate charge is that it is normally drawn from the high voltage input supply. However, power can be saved by obtaining the gate charge from a high efficiency external supply (between 5V and 7V) connected to the EXTV_{CC} pin. This could be the output voltage of the regulator, a boosted version of the output or some other system supply, if available.

Removing Output Voltage Constraints along with R_{SENSE}

The LTC1625 can be configured for a wide variety of output voltages using the V_{PROG} and V_{OSENSE} pins. For basic 3.3V and 5V applications, one can use an internal resistive divider with the output connected directly to the V_{OSENSE} pin. Connect the V_{PROG} pin to INTV_{CC} for a 5V output or to ground for a 3.3V output. Leaving the V_{PROG} pin open disables the internal resistive divider and connects the error-amplifier feedback node directly to the V_{OSENSE} pin. With an external resistive divider, the LTC1625 is capable of regulating an output voltage anywhere between the input voltage and the 1.19V internal reference. This represents a significant improvement over previous current mode controllers, which were constrained by the common mode range of the current sense signal lines.

Start-up and shutdown of the LTC1625 can be controlled via the RUN/SS pin. This pin is connected to an external capacitor that is charged from an internal 3μA current source. The controller will be shut down if this pin is held below 1.4V. After the pin is released, the part stays shut down while the capacitor is charged, permitting a controlled delay for sequencing the power supply start-up. When the voltage rises above 1.4V, the controller will start but with a clamp on the current threshold volt-

age that limits the load current to approximately one third of its maximum value. Limiting the load current reduces the inrush current into the converter. As the voltage increases above 1.4V, the clamp is gradually raised to its normal value.

Design Examples

Figure 3 shows the LTC1625 in an application supplying a 2.5V output using an external feedback divider. Si4410DY MOSFETs from Siliconix allow this converter to deliver up to 5A of load current. Ripple current is 1.8A (36% of full load) and current limit occurs around 6A. Note also that the EXTV_{CC} pin is connected to an external 5V supply. This increases efficiency by drawing the roughly 7mA gate charge current from a supply lower than V_{IN}.

An efficiency plot of this circuit is shown in Figure 4. An LTC1435 with identical components in the power path is also plotted for comparison. At lower output voltages such as this, the sense resistor is responsible for an increasing share of the total power loss. By eliminating this source of loss, the LTC1625 is easily able to deliver an efficiency greater than 90% at high load current. The benefit of reduced I²R loss is readily apparent at the highest loads. The controller makes a transition to Burst Mode operation below around 1.1 A which keeps the efficiency high at moderate loads.

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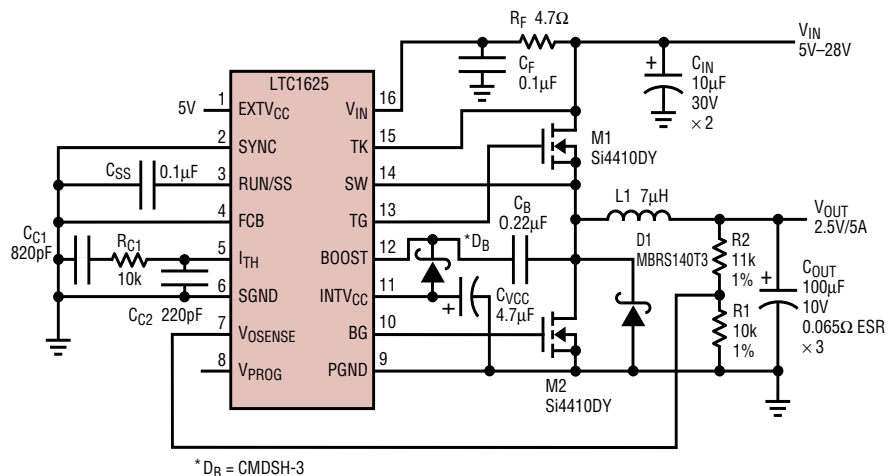


Figure 3. 2.5V/5A adjustable-output supply

LTC1627 Monolithic Synchronous Step-Down Regulator Maximizes Single or Dual Li-Ion Battery Life

by Jaime Tseng

Introduction

The LTC1627 is a new addition to a growing family of power management products optimized for Li-Ion batteries. Li-Ion batteries, with their high energy density, are becoming the chemistry of choice for many hand-held products. As the demand for longer battery operating time continues to increase and the operating voltages of submicron DSPs and microcontrollers decreases, more demands are placed on DC/DC conversion. The LTC1627 monolithic, current mode synchronous buck regulator (Figure 1) was specifically designed to meet these demands.

Single and Double Li-Ion Cell Operation

The LTC1627, with its operating supply range of 2.65V to 8.5V, can operate from one or two Li-Ion batteries as well as 3- to 6-cell NiCd and NiMH battery packs. Figure 2 shows a typical discharge voltage profile of a single

Li-Ion battery. As shown, a fully charged single-cell Li-Ion battery begins the discharge cycle around 4V (it may be slightly higher or lower, depending upon the manufacturer's charge-voltage specifications). During the bulk of the discharge time, the cell produces between 3.5V and 4.0V. Finally, towards the end of discharge, the cell voltage drops quickly below 3V. When the voltage drops further, the discharge must be terminated to prevent damage to the battery. A precision undervoltage lockout circuit trips when the LTC1627's supply voltage dips below 2.5V, shutting the part down to only 5 μ A of supply current.

Maximizing Battery Run Time

The LTC1627 incorporates power saving Burst Mode operation and 100% duty cycle for low dropout to maximize the battery operating time. In Burst Mode operation, both power

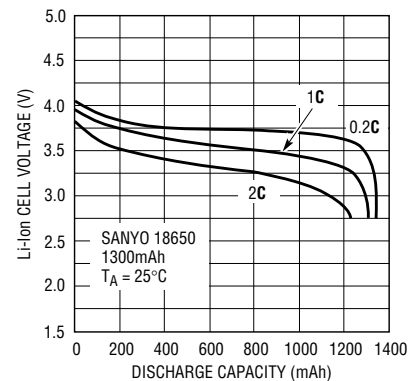


Figure 2. Typical single-cell Li-Ion discharge curve

MOSFETs are turned off for increasing intervals as the load current drops. Along with the gate-charge savings, unused circuitry is shut down between burst intervals, reducing the quiescent current to 200 μ A. This extends operating efficiencies exceeding 90% to over two decades of output load range (see Figure 3). As the battery discharges, the LTC1627 smoothly shifts from a high efficiency switch-mode DC/DC regulator to a low dropout (100% duty cycle) switch. In this mode, the voltage drop between the battery input and the regulator output is determined by the load current, the series resistance of the

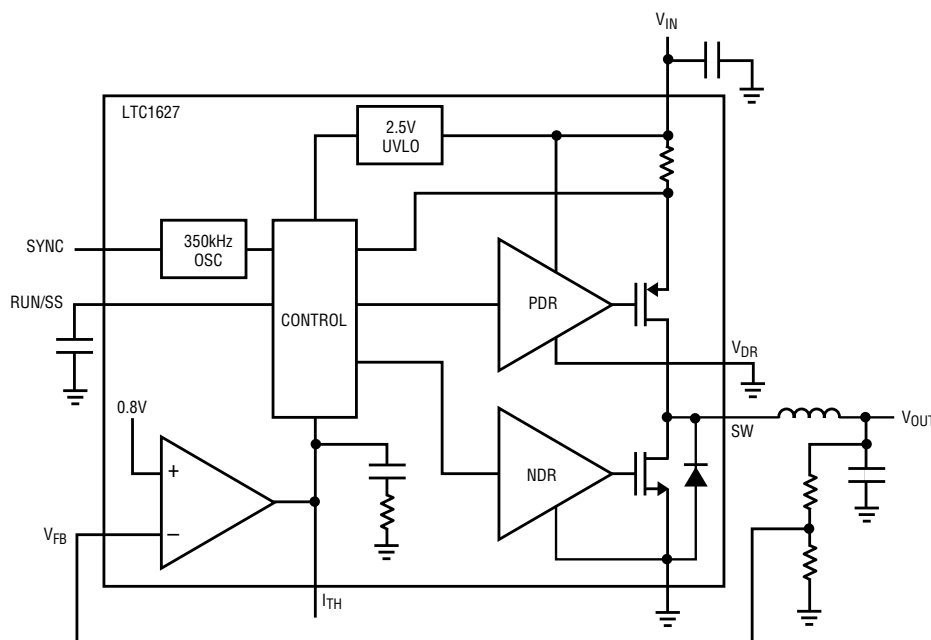


Figure 1. LTC1627 block diagram

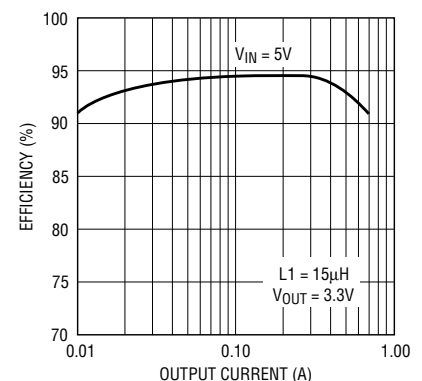


Figure 3. Efficiency vs output load current

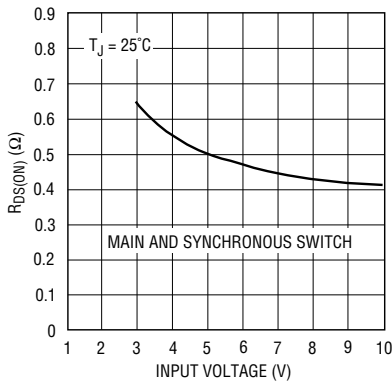


Figure 4. R_{DS(ON)} for both switches vs input voltage

internal P-channel power MOSFET and the inductor resistance.

The internal power MOSFET switches provide very low resistance even at low supply voltages. Figure 4 is a graph of switch resistance vs supply voltage for both switches. The R_{DS(ON)} is typically 0.5Ω at 5V and only rises to approximately 0.65Ω at 3V, for both switches. This low switch R_{DS(ON)} ensures high efficiency switching as well as low dropout DC characteristics at low supply voltages.

Extending Low Supply Operation

At low supply voltages, the LTC1627 is most likely to be running at high duty cycles or in dropout, where the P-channel main switch is on continuously. Hence, the I²R loss is due mainly to the R_{DS(ON)} of the P-channel MOSFET. When V_{IN} is below 4.5V, the R_{DS(ON)} of the P-channel MOSFET can be lowered further by driving its gate below ground. The top P-channel MOSFET driver makes use of a floating return pin, V_{DR}, to allow biasing below

GND. A simple charge pump bootstrapped to the SW pin realizes a negative voltage at the V_{DR} pin, as shown in Figure 5. Each time the SW node cycles from low to high and then from high to low, charge is transferred from C2 to C1 producing a negative voltage at V_{DR} equal in magnitude to V_{IN} - (2 • V_{DIODE}). In dropout, when the P-channel MOSFET is turned on continuously, a dropout detector counts the number of oscillator cycles that the P-channel MOSFET remains on and periodically forces a brief off period to allow C1 to recharge. When 100% duty cycle is desired, V_{DR} can be grounded to disable the dropout detector.

Constant-Frequency, Current Mode Architecture

The LTC1627 uses a constant-frequency, current mode step-down architecture that provides excellent rejection of input line and output load transients and also provides cycle-by-cycle current limiting. Input line transients are rejected by the feed-forward characteristics inherent in current mode control. The output load transients are rejected by the greater error-amplifier bandwidth afforded in current mode control. In current mode, the circuit behaves as if there were a constant current feeding the parallel combination of the output capacitor and output load, yielding only a 90° rather than a 180° phase lag. This simplifies the feedback-loop design and the circuitry around the error amplifier required for stabilization.

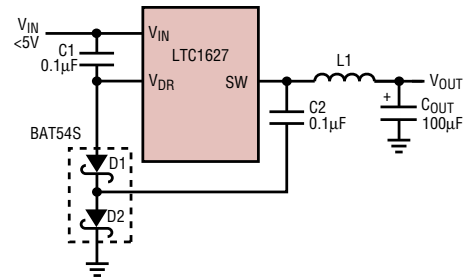


Figure 5. Using a charge pump to bias V_{DR}

Current mode limits the peak current cycle-by-cycle, protecting the internal main switch and synchronous rectifier. In extreme cases, when the output is shorted to ground, the frequency of the oscillator is reduced to one-tenth of its nominal frequency to allow the inductor current time to decay and prevent inductor-current runaway. The oscillator's frequency gradually increases back to its nominal frequency when V_{FB} rises above 0.3V.

The internal oscillator is set for a fixed switching frequency of 350kHz, allowing the use of small surface mount inductors. In switching-noise-sensitive applications, the LTC1627 can be externally synchronized to frequencies of up to 525kHz. During synchronization, Burst Mode operation is inhibited and pulse-skipping mode is used. In this mode, when the output load is very low, the current comparator remains tripped for more than one cycle and forces the main switch to stay off for the same number of cycles. Increasing the output load slightly allows constant frequency PWM operation to resume.

Minimal External Components

Size is extremely important in modern portable electronics, so the LTC1627 is designed to work with a minimum number of external components. The loop compensation, current sense resistor and the main and synchronous switches are internal. An internal catch diode is also provided across the internal synchronous switch, eliminating parasitic currents or latch-up if the external Schottky diode is omitted. Only an

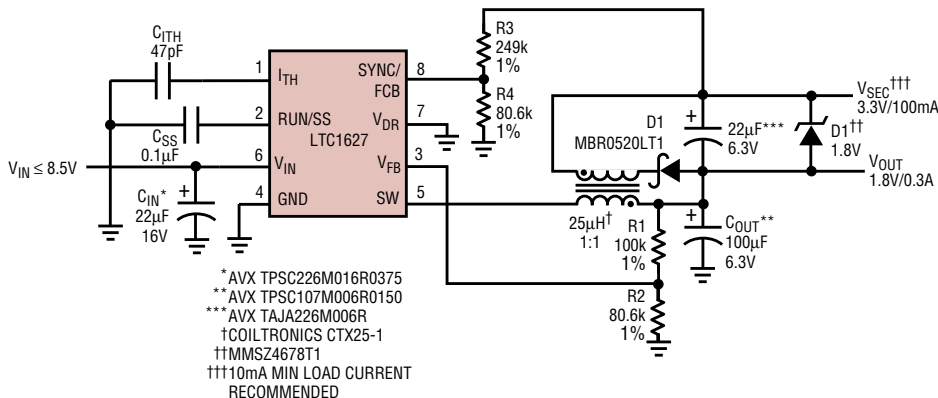


Figure 6. Dual-output 1.8V/0.3A and 3.3V/100mA application

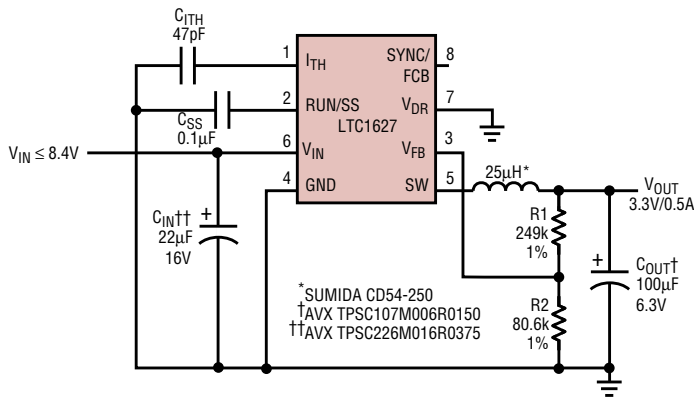


Figure 7. Dual lithium-ion to 3.3V/0.5A regulator

Typical Applications


1 or 2 Li-Ion Step-Down Converter

Figure 7 is a schematic diagram showing the LTC1627 being powered by one or two Li-Ion batteries. All the components shown in this schematic are surface mount and have been selected to minimize the board space and height. The output voltage is set at 3.3V, but is easily programmed to other voltages.

Single Li-Ion Step-Down Converter

The circuit in Figure 8 is intended for input voltages below 4.5V, making it ideal for single Li-Ion battery applications. Diodes D1 and D2 and capacitors C1 and C2 comprise the bootstrapped charge pump to realize a negative supply at the V_{DR} pin, the return pin for the top P-channel MOSFET driver. This allows Figure 8's circuit to maintain low switch $R_{DS(ON)}$ all the way down to the UVLO trip voltage.

Conclusion

The new LTC1627 monolithic synchronous buck regulator is a versatile, high efficiency, DC/DC converter that is at home in a wide range of low input voltage applications. Features such as precision UVLO and optional bootstrapped gate drive make it particularly well suited to single-cell Li-Ion power. 

inductor, input and output filter capacitors and two small resistors and capacitors are needed to construct a high efficiency DC/DC switching regulator (see Figure 7). The 47pF filter capacitor connected to the I_{TH} pin (error-amplifier output) filters out switching noise. If the loop compensation needs to be adjusted for a specific application, the I_{TH} pin can also be used for external compensation.

Auxiliary-Winding Control Using the SYNC/FCB Pin

Besides higher efficiency and lower switching noise, synchronous switching provides a means of regulating a secondary flyback winding. In non-synchronous regulators, power must

be drawn from the inductor primary winding in order to extract power from auxiliary windings. But with continuous synchronous operation, power can be drawn from the auxiliary windings without regard to the primary output load.

The LTC1627, with its synchronous switching and attendant circuitry, provides the means of easily constructing a secondary flyback regulator, as shown in Figure 6. This flyback regulator is regulated by the secondary feedback resistive divider tied to the SYNC/FCB pin. This pin forces continuous operation whenever it drops below its ground-referenced threshold of 0.8V. Power can then be drawn from the secondary flyback regulator whether the main output is loaded or not.

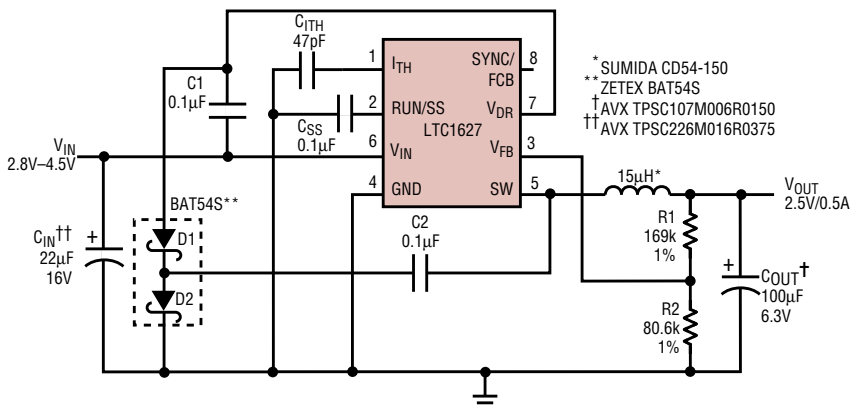


Figure 8. Single lithium-ion to 2.5V/0.5A regulator



Clock-Tunable, High Accuracy, Quad 2nd Order, Analog Filter Building Blocks

by Philip Karantzalis

Introduction

The LTC1068 product family consists of four monolithic, clock-tunable filter building blocks. Each product contains four matched, low noise, high accuracy 2nd order switched capacitor filter sections. An external clock tunes the center frequency of each 2nd order filter section. The LTC1068 products differ only in their clock-to-center frequency ratio. The clock-to-center frequency ratio is set to 200:1 (LTC1068-200), 100:1 (LTC1068), 50:1 (LTC1068-50) or 25:1 (LTC1068-25). External resistors can modify the clock-to-center frequency ratio. High precision, high performance, quad 2nd order, dual 4th order or single 8th order filters can be designed with an LTC1068 family product. Designing filters with an LTC1068 product is fully supported by the FilterCAD™ 2.0 design soft-

ware for Windows®. The internal sampling rate of all the LTC1068 devices is twice the clock frequency. This allows the frequency of input signals to approach twice the clock frequency before aliasing occurs. Maximum clock frequency for LTC1068-200, LTC1068 and LTC1068-25 is 6MHz with ±5V supplies; that for the LTC1068-50 is 2MHz with a single 5V supply. For low power filter applications, the LTC1068-50 power supply current is 4.5mA with a single 5V supply and 2.5mA with a single 3V supply. The LTC1068 products are available in a 28-pin SSOP surface mount package. The LTC1068 (the 100:1 part) is also available in a 24-pin DIP package. The following four circuits are typical examples of application-specific filters that the LTC1068 products can realize.

LTC1068-200 Ultralow Frequency Linear-Phase Lowpass Filter

Figure 1 shows an LTC1068-200 linear-phase 1Hz lowpass filter schematic and Figure 2 shows its gain and group delay responses. The clock frequency of this filter is 400 times the -3dB frequency (f_{-3dB} or f_{CUTOFF}). The large clock-to- f_{CUTOFF} frequency ratio of this filter is useful in ultralow frequency filter applications when minimizing aliasing errors could be an important consideration. For example, the 1Hz lowpass filter shown in Figure 1 requires a 400Hz clock frequency. For this filter, the input frequencies that can generate aliasing errors are in a band from 795Hz to 805Hz ($2 \times f_{CLK} \pm 5 \times f_{-3dB}$). For most very low frequency signal-processing applications, the signal spectrum is less than 100Hz. Therefore, Figure 1's filter will process very low frequency signals without significant aliasing errors, since its clock frequency is 400Hz and the aliasing inputs are in a small band around 800Hz.

Windows is a registered trademark of Microsoft Corp.

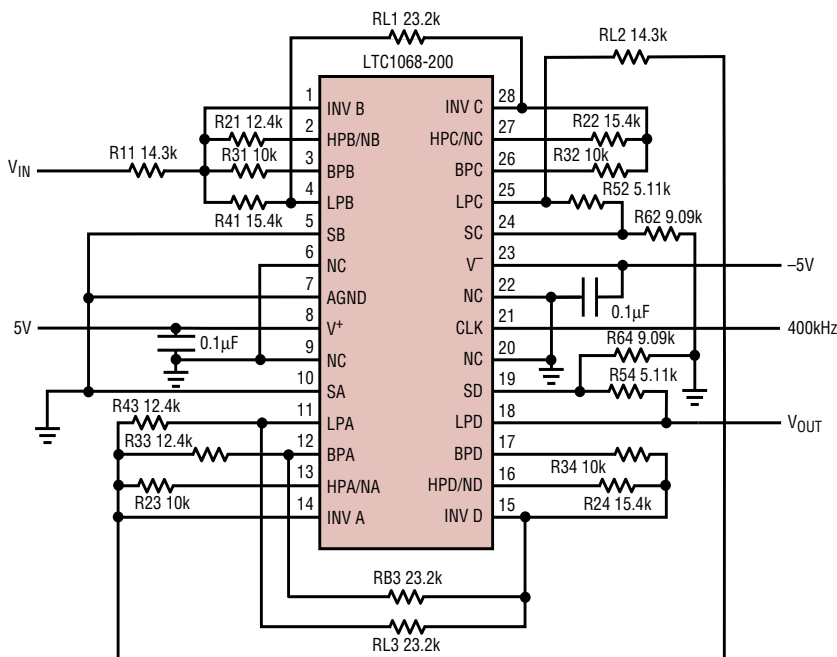


Figure 1. Linear-phase lowpass filter: $f_{-3dB} = 1\text{Hz} = f_{CLK}/400$

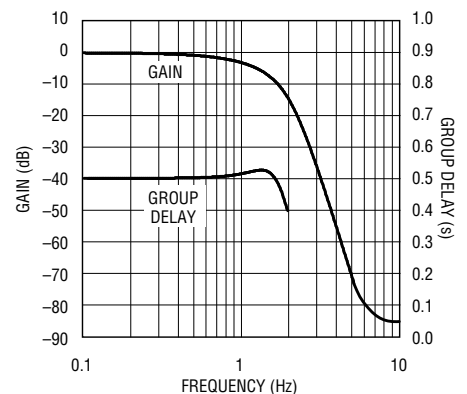


Figure 2. Gain and group delay response of Figure 1's circuit.

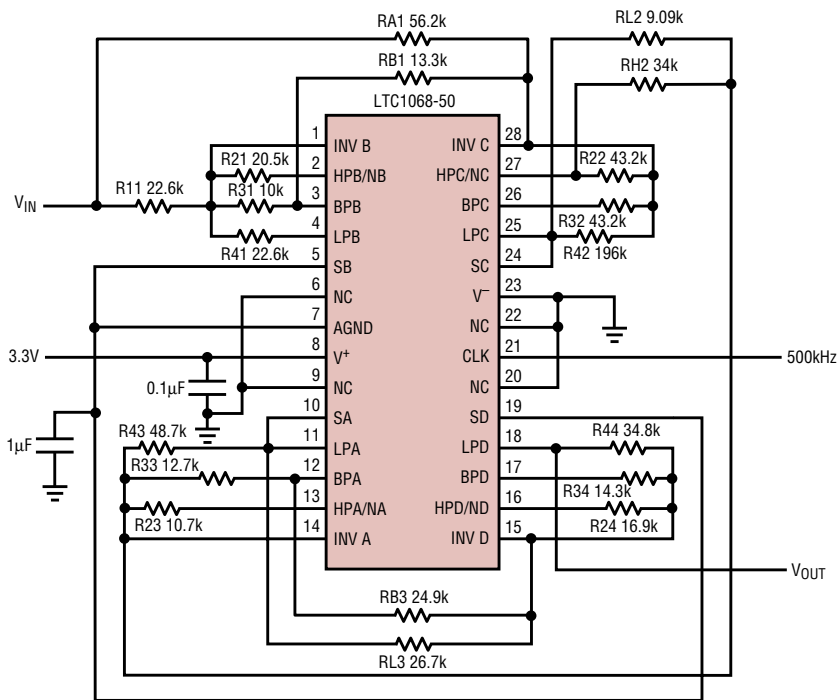


Figure 3. Low power, single 3.3V supply, 10kHz, 8th order, linear-phase lowpass filter

LTC1068-50 Single 3.3V Low Power Linear-Phase Lowpass Filter

Figure 3 is a schematic of an LTC1068-50-based, single 3.3V, low power, lowpass filter with linear phase. The clock-to- f_{CUTOFF} ratio is 50 to 1 (f_{CUTOFF} is the -3dB frequency). Figure 4 shows the gain and group delay response.

The flat group delay response in the filter's passband implies a linear phase. A linear-phase filter has a transient response with very small overshoot that settles very rapidly. A linear-phase lowpass filter is useful for processing communication signals with minimum intersymbol interference in digital communications transmitters or receivers. The

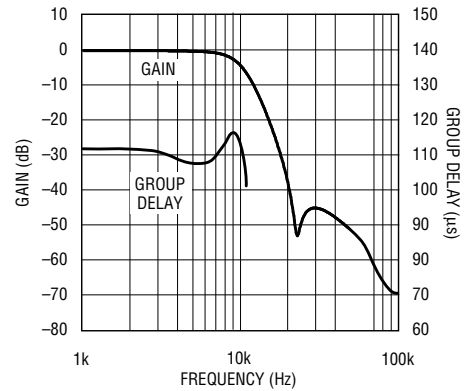


Figure 4. Gain and group delay response of Figure 3's filter

maximum clock frequency for this filter is 1MHz with a single 3.3V supply and 2MHz with a single 5V supply. Typical power supply current is 3mA with a single 3.3V supply and 4.5mA with a single 5V supply.

LTC1068-25 Selective Bandpass Filter is Clock Tunable to 80kHz

Figure 5 shows a 70kHz bandpass filter based on the LTC1068-25 operating with dual 5V power supplies. The clock-to-center frequency ratio is 25 to 1. Figure 6 shows the gain response of Figure 5's bandpass filter. The passband of this filter extends from $0.95 \times f_{CENTER}$ to $1.05 \times f_{CENTER}$. The stopband attenuation is greater than 40dB at $0.8 \times f_{CENTER}$ and $1.15 \times f_{CENTER}$. The center frequency can be clock tuned to 80kHz with dual 5V supplies and to 40kHz with a single 5V supply. With FilterCAD, the LTC1068-25 can be used to realize bandpass filters less selective than that shown in Figure 6, which can be clock tuned up to 160kHz with dual 5V supplies.

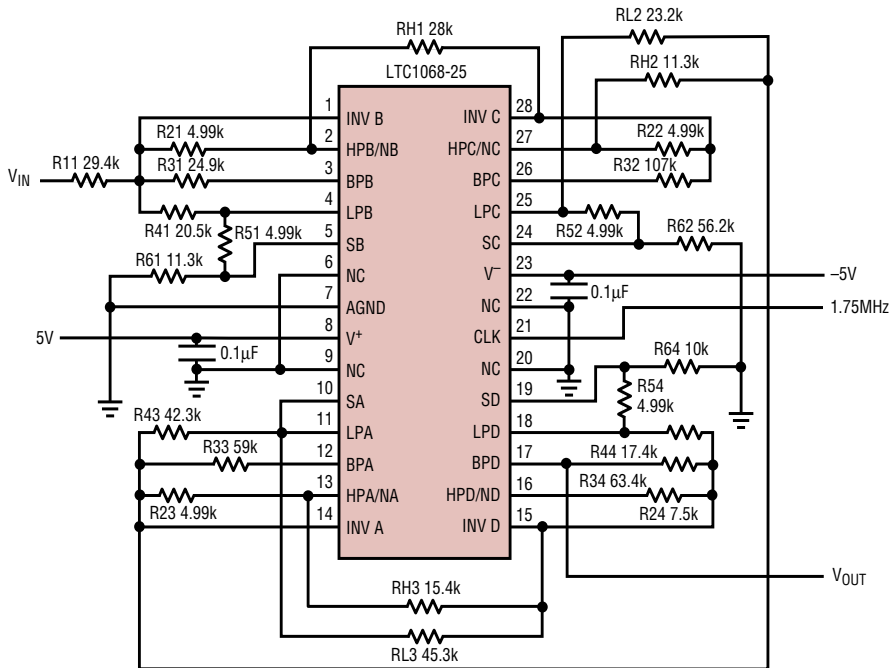


Figure 5. 70kHz, 8th order, bandpass filter

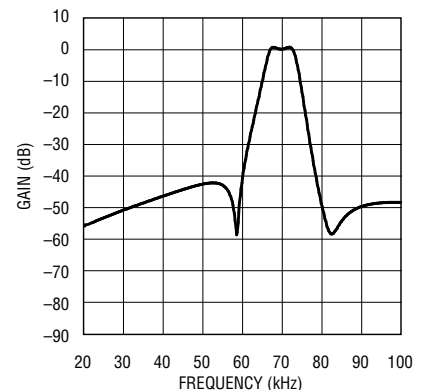


Figure 6. Gain response of Figure 5's filter

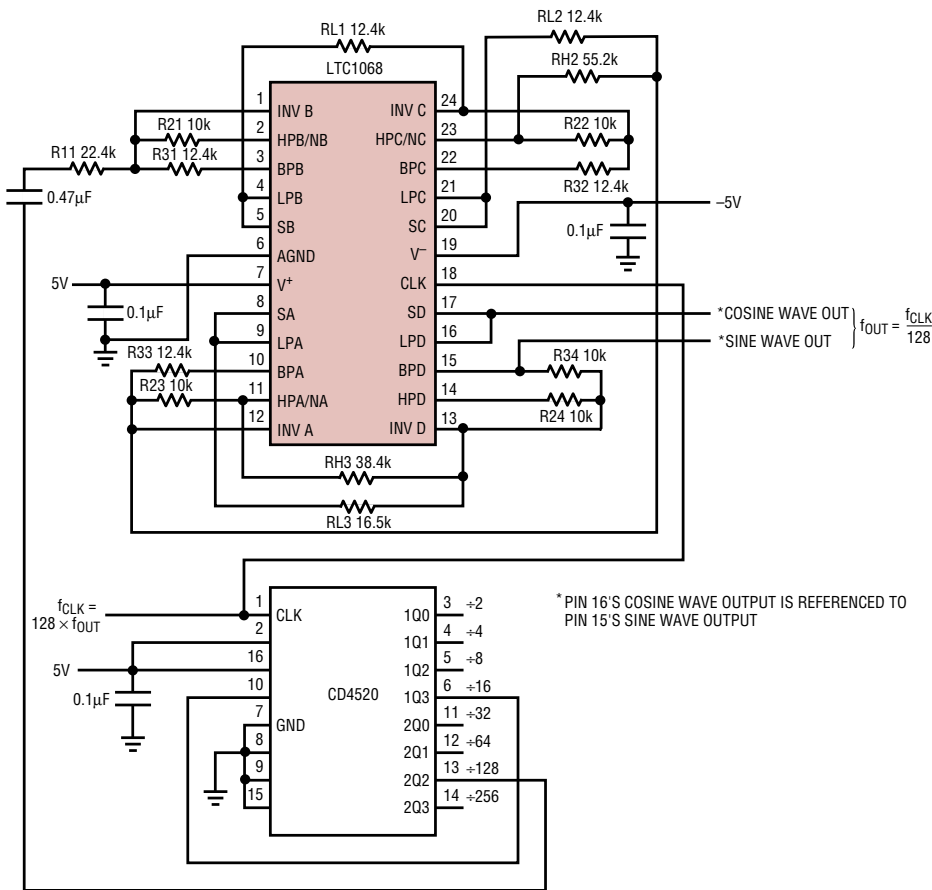


Figure 7. Square-wave-to-quadrature oscillator converter

LTC1068 Square-Wave-to-Quadrature Oscillator Filter

Figure 7 shows the schematic of a LTC1068 based filter that is specifically designed to produce a low harmonic distortion sine and cosine oscillator from a CMOS-level square wave input. The reference sine wave output of Figure 7’s circuit is on pin 15 (BPD on the 24-pin LTC1068 package) and the cosine output is on pin 16 (LPD on the 24-pin LTC1068 package). The output frequency of this quadrature oscillator is the filter’s clock frequency divided by 128. The output of a CMOS CD4520 divide-by-128 counter is coupled with a 0.47µF capacitor to the input to the LTC1068 filter operating with dual 5V power supplies. The filter’s clock frequency is the input to the CD4520 counter.

The LTC1068 filter is designed to pass the fundamental frequency component of a square wave and attenuate any harmonic components higher than the fundamental. An ideal square wave (50% duty cycle) will have only odd harmonics (3rd, 5th, 7th and so on), whereas a typical practical square wave has a duty cycle less or more than 50% and will also have even harmonics (2nd, 4th, 6th and so on). The filter of Figure 7 has a stopband notch at the 2nd and 3rd harmonics for a square wave input with a frequency equal to the filter’s clock frequency divided by 128. The filter’s sine wave output (pin 15) is 1V_{RMS} for a ±2.5V square wave input and has less than 0.025% THD (total harmonic distortion) for input frequencies up to 16kHz and less than 0.1% THD

for frequencies up to 20kHz. The cosine output (on pin 16, referenced to pin 15’s sine wave output) is 1.25V_{RMS} for a ±2.5V square wave input and has less than 0.07% THD for frequencies up to 20kHz.

The 20kHz frequency limit is due to the CD4520; with a 74HC type divide-by-128 counter, sine and cosine waves up to 40kHz can be generated with the LTC1068-based filter of Figure 7.

The LTC1068 Product Family: Versatile Filter Building Blocks, 1Hz to 200kHz

The previous four filter examples are typical of the great variety of filters that can be designed with the LTC1068 product family. As a general selection guide, the following is recommended: for low noise and low frequency filters less than 20kHz, use the LTC1068-200; for low noise and low frequency filters less than 40kHz, use the LTC1068; for low power filters up to 20kHz operating with single 3V to 5V supplies, the LTC1068-50 should be the choice; and for filters in the frequency range 40kHz to 200kHz, use the LT1068-25. The FilterCAD design software will recommend the appropriate LTC1068 device for most filter applications. For some application-specific filter designs, the choice of the proper LTC1068 device may not be obvious and the assistance of a Linear Technology applications engineer will be helpful.

LTC1068-Based Semicustom Filters

For application-specific filter requirements of single 8th order or dual 4th order filters, a customized version of an LTC1068-family product can be obtained in a 16-pin SO package with internal thin-film resistors. Clock-to-center frequency ratios higher or lower than 200:1, 100:1, 50:1 or 25:1 can also be obtained. Please contact LTC Marketing for details.

Authors can be contacted at (408) 432-1900

New DC/DC Controller Enables High Step-Down Ratios

by Greg Dittmer

Importance of Minimum On-Time

As processor voltage requirements are pushed lower and lower, input supply voltages remain high, forcing DC/DC converters to operate at lower and lower duty cycles. Since operating frequencies also remain high to minimize noise and the size of components, the on-time of the topside switch in a constant-frequency converter must continue to decrease to regulate the lower and lower output voltages. The required on-time is given by $T_{ON} = V_{OUT}/(V_{IN} \cdot f)$

Unfortunately, there is a limit to how small this time can be. In a typical current mode DC/DC converter, once the main switch is turned on at the beginning of each switching cycle, the speed at which it can be turned off is limited by the response time of the current comparator, the time required for the turn-off command to propagate through the logic and output driver and the time required to discharge the capacitance of the topside gate. These delays add up to a few hundred nanoseconds and constitute the minimum time the topside switch must stay on during each switching cycle. If the maximum V_{IN} and frequency are fixed, this minimum on-time sets a lower limit on

output voltage. If an output voltage below this limit is required, the only choice is to lower the operating frequency, which is usually not desirable. Figure 1 shows the on-times required with $V_{IN} = 22V$ as a function of output voltage for various frequencies.

Capabilities of the LTC1435

The LTC1435 high efficiency synchronous DC/DC controller has been extremely popular for notebook computers and other battery-powered equipment due to its low noise, constant-frequency operation and its dual N-channel drive for outstanding high current efficiency without sacrificing low dropout operation. However, its 400ns–500ns minimum on-time requires lower operating frequencies (<150kHz) to regulate output voltages below 2.0V if V_{IN} is high.

What happens if minimum on-time is violated in the LTC1435? If V_{IN} is increased so that the on-time falls below $T_{ON(MIN)}$, the LTC1435 will begin to skip cycles to remain in regulation. During this “cycle-skipping” mode, the output remains in regulation but the operating frequency decreases, causing the inductor ripple current and output ripple voltage to increase.

Enter the LTC1435A

The operating envelope has been substantially expanded with the introduction of the new LTC1435A DC/DC controller, which has all the outstanding features of the LTC1435 with a reduced minimum on-time of 300ns or less and improved noise immunity at low output voltages. With these improvements, high performance at output voltages down to 1.3V can be achieved with operating frequencies in excess of 250kHz from input supply voltages above 22V. Figure 2 shows the resulting improvement of maximum V_{IN} vs output voltage as a result of the reduced minimum on-time.

The LTC1435A’s minimum on-time is dependent on the speed of the internal current comparator, which in turn is dependent on the amplitude of the signal the comparator is monitoring: inductor ripple current. Thus, the higher the ripple current, the lower the minimum on-time. Figure 3 shows how minimum on-time varies as a function of the inductor ripple amplitude. At higher amplitudes, $T_{ON(MIN)}$ is less than 250ns; at low amplitudes it can be 350ns or more. This means that for low duty cycle applications where the on-time

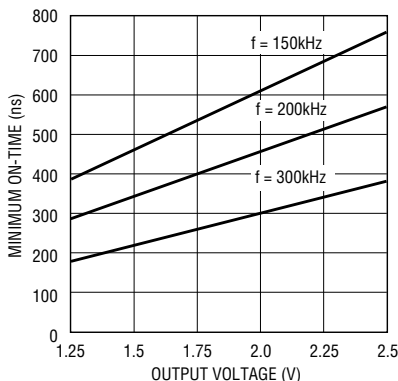


Figure 1. Minimum on-time required for $V_{IN} = 22V$

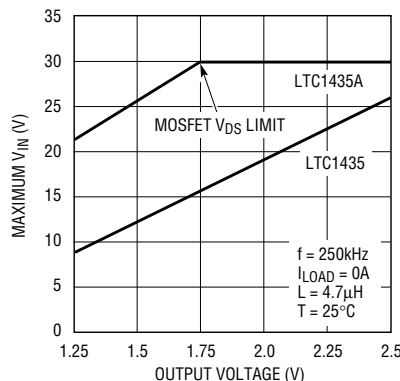


Figure 2. LTC1435/LTC1435A maximum V_{IN} comparison

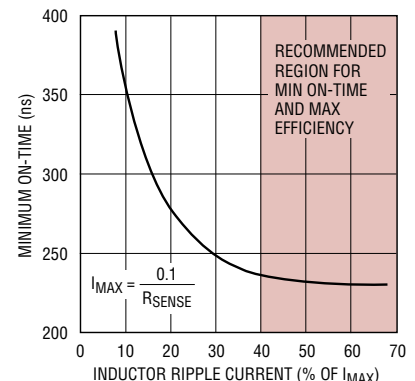


Figure 3. LTC1435A minimum on-time vs inductor ripple current

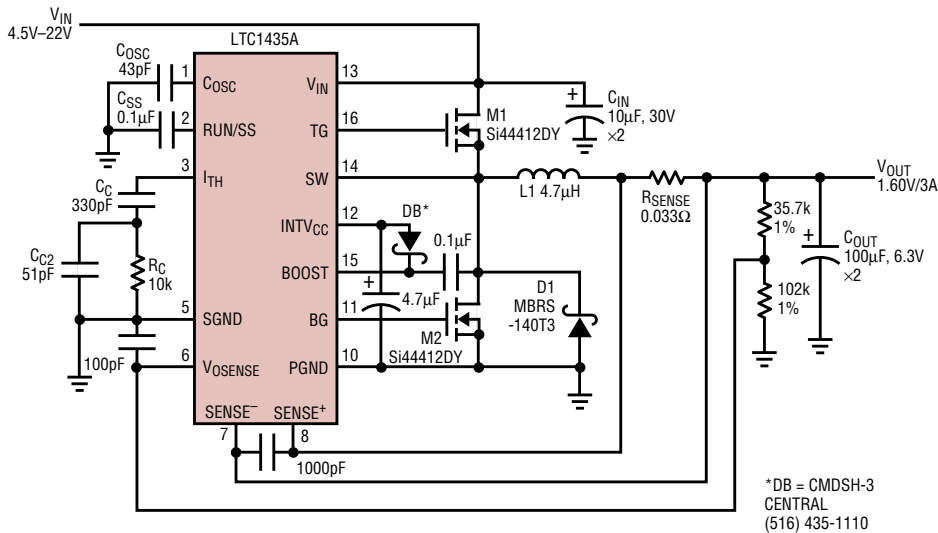


Figure 4. LTC1435A 22V to 1.6V/3A converter (f = 250kHz)

is approaching $T_{ON(MIN)}$, there may be a minimum ripple current amplitude, and hence, a maximum inductance necessary to prevent cycle skipping. Or, expressed differently, the lower the inductance, the higher the maximum V_{IN} that can be achieved before the minimum on-time is violated and cycle skipping occurs. For most applications, 40% ripple not only reduces the minimum on-time but also optimizes efficiency.

22V to 1.6V Converter at 250kHz

Figure 4 shows the LTC1435A configured in an all N-channel synchronous buck topology as a 22V to 1.6V/3A converter running at 250kHz. The 43pF C_{OSC} capacitor sets the internal

oscillator frequency at 250kHz and the 33mΩ sense resistor sets the maximum load current at 3A. For a 22V to 1.6V converter, the on-time required is:

$$T_{ON} = 1.6 / (22 \times 250kHz) = 291ns$$

Can the LTC1435A do this? At maximum V_{IN} the inductor ripple is

$$\begin{aligned} \Delta I_L &= \frac{V_{OUT} \cdot (1 - V_{OUT}/V_{IN})}{F \cdot L} \\ &= \frac{1.6 \cdot (1 - 1.6/22)}{250kHz \cdot 4.7\mu H} = 1.3A \end{aligned}$$

which is 43% of the 3A maximum load. From Figure 3, 43% ripple gives a minimum on-time of 235ns, which is well below the 291ns required by

this application, so no cycle skipping will occur. If a 10μH inductor is used, the ripple amplitude drops to 0.6A or 20% and the minimum on-time increases to 280ns. This does not provide much margin below the 291ns on-time required, and thus the 4.7μH inductor is a better choice.

Intel Mobile Processor VID Power Converter

Figure 5 shows the LTC1435A used with an LTC1706-19 to implement an Intel Mobile Pentium® II Processor VID power converter. This DC/DC converter provides digitally selectable output voltages over the range of 1.3V to 2.0V in 50mV increments at 250kHz and a 7A load current. The selectable output voltage is implemented by replacing the conventional feedback resistor network with the LTC1706-19, which provides the appropriate feedback resistor ratios internally (see the accompanying article in this issue). The proper ratio is selected with the 4-bit digital input pins.

Conclusion

The LTC1435A retains all the outstanding features of the LTC1435, such as constant-frequency operation, dual N-channel MOSFET drive and low dropout, while adding enhancements such as reduced minimum on-time and improved performance at low output. With these enhancements, the LTC1435A is a perfect fit for notebook computers and battery-powered equipment requiring high frequency, low duty cycle DC/DC converters.

Pentium is a registered trademark of Intel Corp.

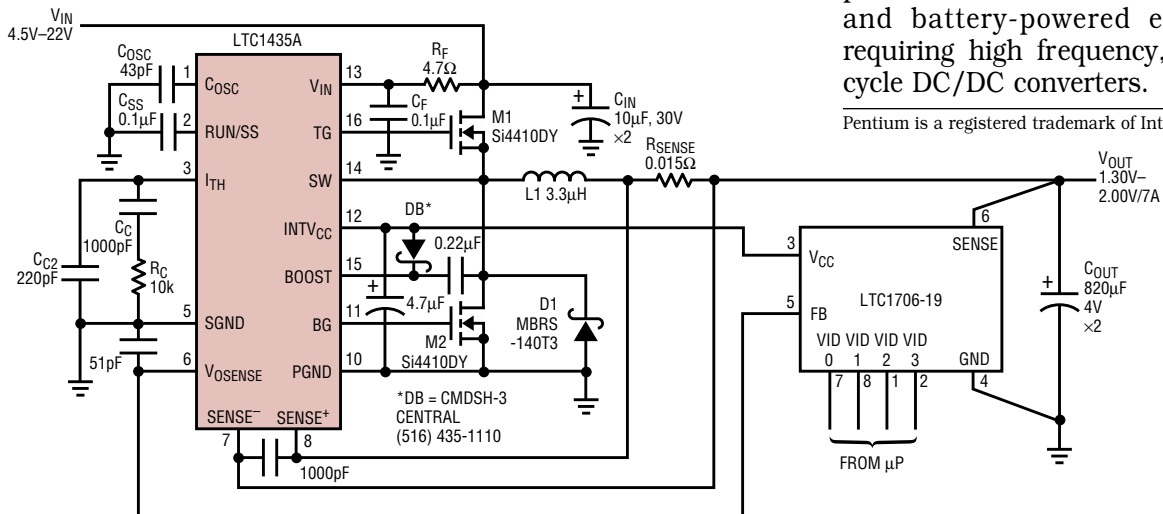


Figure 5. Intel Mobile Pentium II processor VID power converter

VID Voltage Programmer for Intel Mobile Processors

by Peter Guan

Microprocessor manufacturers' relentless push for higher speed and lower power dissipation, especially in areas of mobile laptop computer processors, is forcing supply voltages to these processors to a level previously thought impossible or impractical. In fact, the supply voltage has become so critical that different microprocessors demand different yet precise supply voltage levels in order to function optimally.

To accommodate this new generation of microprocessors, LTC introduces the LTC1706-19 VID (voltage identification) voltage programmer. This device is a precision, digitally programmable resistive divider designed for use with an entire family of LTC's DC/DC converters with onboard 1.19V references. These converters include the LTC1433, LTC1434, LTC1435, LTC1435A, LTC1436, LTC1438, LTC1439, LTC1538-AUX, LTC1539 and LTC1624. (Consult the factory for future compatible DC/DC converter

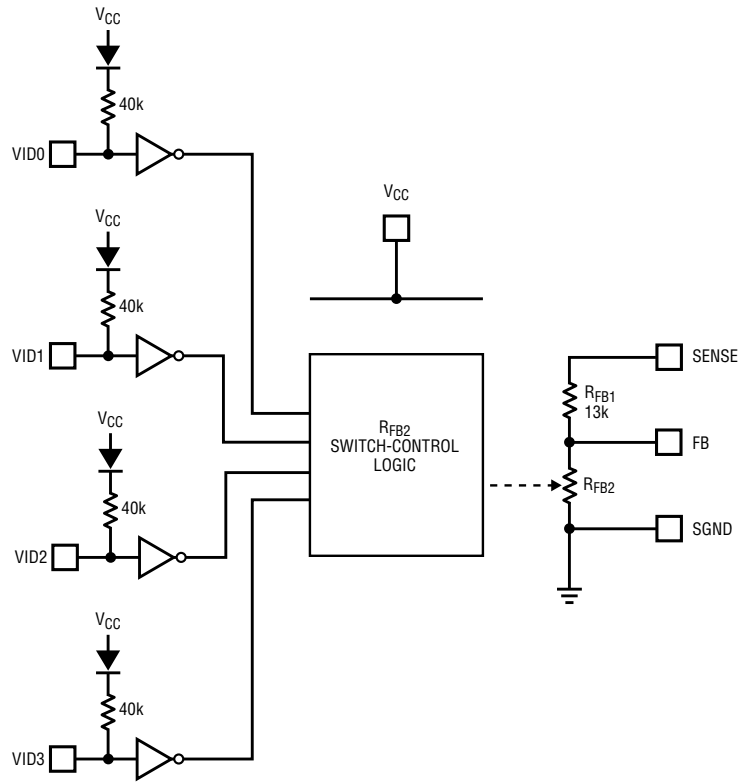


Figure 2. LTC1706-19 block diagram

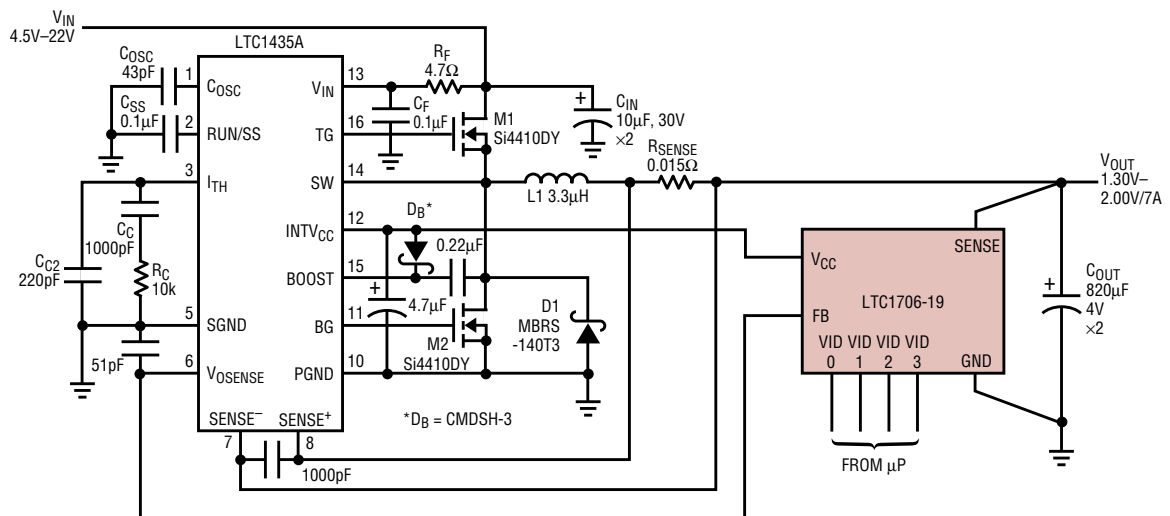


Figure 1. Intel Mobile Pentium II processor VID power converter

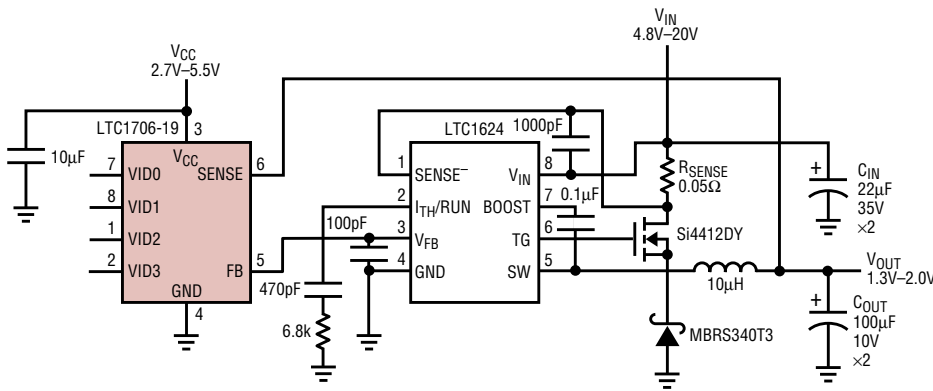


Figure 3. High efficiency SO-8, N-channel switching regulator with programmable output

products.) The LTC1706-19 is fully compliant with the Intel mobile VID specifications and comes in a tiny SO-8 package. Four digital pins are provided to program output voltages from 1.3V to 2.0V in 50mV steps with an accuracy of $\pm 0.25\%$.

Figure 1 shows a VID-programmed DC/DC converter for an Intel mobile processor that uses the LTC1435A and LTC1706-19 to deliver 7A of output current with a programmable V_{OUT} of 1.3V to 2.0V from a V_{IN} of 4.5V to 22V. Simply connecting the LTC1706-19's FB and SENSE pins to the LTC1435A's V_{OSENSE} and SENSE⁻ pins, respectively, closes the loop between the output voltage sense and the feedback inputs of the LTC1435A regulator with the appropriate resistive divider network, which is controlled by the LTC1706-19's four VID input pins.

Figure 2 shows a simplified block diagram of the LTC1706-19. A 40k resistor in series with a diode from V_{CC} pulls up each VID input pin. Therefore, the VID pin must be grounded or driven low to produce a digital low input, whereas a digital high input can be generated by either floating the VID pin or connecting it to V_{CC} . Series diodes from V_{CC} are included to prevent the inputs from being damaged or clamped by a potential higher than V_{CC} . This allows the LTC1706-19 to be fully TTL compatible and operational over a VID input voltage range that is much higher than V_{CC} . When all the inputs are high, the LTC1706-19 has a typi-

cal quiescent current of 0.1 μ A from V_{CC} , because all active devices are turned off. However, due to the pull-up resistors on each of the VID programming inputs, each grounded input contributes approximately 68 μ A, $(V_{CC} - 0.6)/40k$ of supply current in a 3.3V system.

The top feedback resistor in the block diagram, R_{FB1} , connected between SENSE and FB, is a 15k resistor whose value is not modified by the state of the VID program inputs. The bottom feedback resistor, R_{FB2} , however, is modified by the four VID

inputs. The precision of the ratio between R_{FB2} and R_{FB1} results in a $\pm 0.25\%$ output accuracy.

Table 1 shows the VID inputs and their corresponding output voltages. VID3 is the most significant bit (MSB) and VID0 is the least significant bit (LSB). When all four inputs are low, the LTC1706-19 sets the regulator output voltage to 2.00V. Each increasing binary count is equivalent to decreasing the output voltage by 50mV. Therefore, to obtain a 1.30V output, the three MSBs are left floating while only VID0 is grounded. In cases where all four VID inputs are tied high or left floating, such as when no processor is present in the system, a regulated 1.25V output is generated at V_{SENSE} .

Figure 3 shows a combination of the LTC1624 and the LTC1706-19 configured as a high efficiency step-down switching regulator with a programmable output of 1.3V to 2.0V from an input of 4.8V to 20V. Using only one N-channel power MOSFET, the two SO-8 packaged LTC parts offer an extremely versatile, efficient, compact regulated power supply.

Table 1. VID inputs and corresponding output voltages


Code	VID3	VID2	VID1	VID0	Output
0000	GND	GND	GND	GND	2.00V
0001	GND	GND	GND	Float	1.95V
0010	GND	GND	Float	GND	1.90V
0011	GND	GND	Float	Float	1.85V
0100	GND	Float	GND	GND	1.80V
0101	GND	Float	GND	Float	1.75V
0110	GND	Float	Float	GND	1.70V
0111	GND	Float	Float	Float	1.65V
1000	Float	GND	GND	GND	1.60V
1001	Float	GND	GND	Float	1.55V
1010	Float	GND	Float	GND	1.50V
1011	Float	GND	Float	Float	1.45V
1100	Float	Float	GND	GND	1.40V
1101	Float	Float	GND	Float	1.35V
1110	Float	Float	Float	GND	1.30V

Figure 4 shows the LTC1436A-PLL and the LTC1706-19, a combination that yields a high efficiency low noise synchronous step-down switching regulator with programmable output with programmable 1.3V to 2V outputs and external frequency synchronization capability.

Besides the LTC family of 1.19V-referenced DC/DC converters, the LTC1706-19 can also be used to pro-

gram the output voltages of regulators with different onboard references. Figure 5 shows the LTC1706-19 programming the output of the LT1575, an UltraFast™ transient response, low dropout regulator that is ideal for today's power-hungry desktop microprocessors. However, since the LT1575 has a 1.21V reference instead of a 1.19V reference, the out-

put will range from 1.27V to 2.03V in steps of 50.8mV.

The LTC1706-19 is the ideal companion chip to provide precise, programmable low-voltage outputs for an entire family of LTC DC/DC converters. Its compact size, compatibility and high accuracy are just the right features for today's portable electronic equipment. 

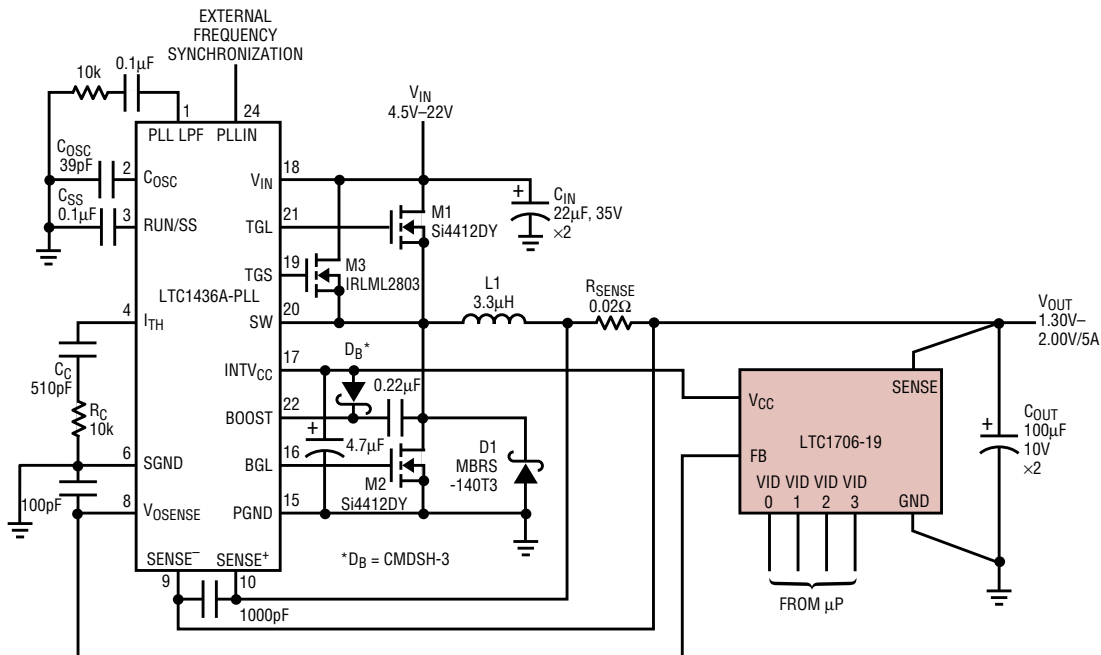


Figure 4. High efficiency, low noise, synchronous step-down switching regulator with programmable output and external synchronization

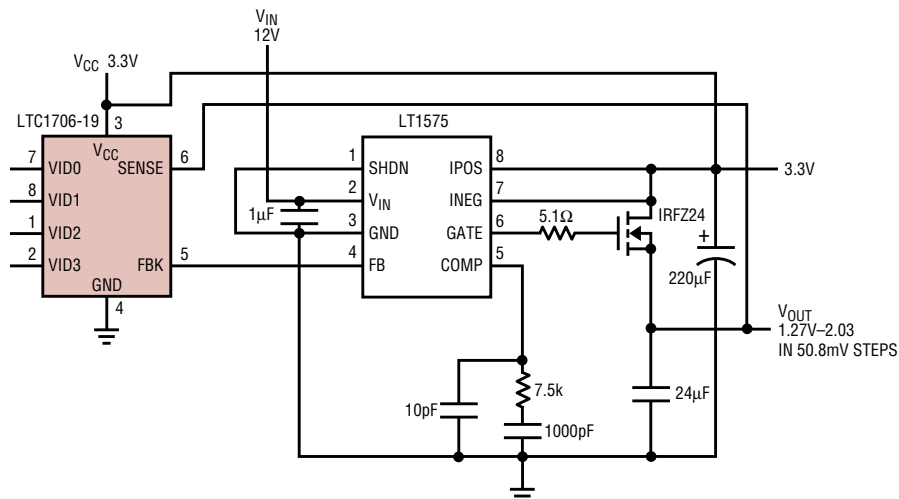


Figure 5. UltraFast transient response, low dropout regulator with adjustable output voltage

Fixed Frequency, 500kHz, 4.5A Step-Down Converter in an SO-8 Operates from a 5V Input

by Karl Edwards

Introduction

The LT1506 is a 500kHz monolithic buck mode switching regulator, functionally identical to the LT1374 but optimized for lower input voltage applications. Its high 4.5A switch rating makes this device suitable for use as the primary regulator in small to medium power systems. The small SO-8 footprint and input operating range of 4V to 15V is ideal for local onboard regulators operating from 5V or 12V system supplies. The 4.5A switch is included on the die, along with the necessary oscillator, control and logic circuitry to simplify design. The part's high switching frequency allows a considerable reduction in the size of external components, providing a compact overall solution.

The LT1506 is available in standard 7-pin DD and fused-lead SO-8 packages. It maintains high efficiency over a wide output current range by keeping quiescent supply current to 4mA and by using a supply-boost capacitor to saturate the power switch. The topology is current mode for fast transient response and good loop stability. Full cycle-by-cycle short-circuit protection and thermal shutdown are provided. Both fixed 3.3V and adjustable output voltage parts are available.

5V to 3.3V Buck Converter

The circuit in Figure 1 is a step-down converter suitable for use as a local regulator to supply 3.3V logic from a 5V power bus. The high efficiency, shown in Figure 2, removes the need for bulky heat sinks or separate power devices, allowing the circuit to be placed in confined locations. Since the boost circuit only needs 3V to operate, the boost diode can still be connected to the output, improving efficiency. Figure 1's circuit shows the shutdown pin option. If this pin is

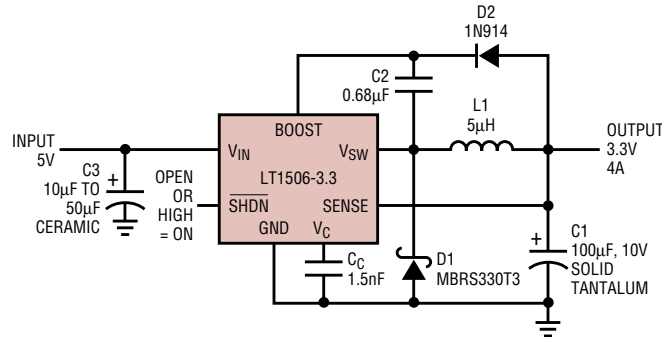


Figure 1. 5V to 3.3V step-down converter

pulled to a logic low, the output is disabled and the part goes into shutdown mode, reducing supply current to 20µA. An internal pull-up ensures correct operation when the pin is left open. The SYNC pin, an option for the DD package, can be used to synchronize the internal oscillator to a system clock. A logic-level clock signal applied to the SYNC pin can synchronize the switching frequency in the range of 580kHz to 1MHz.

Current Sharing Multiphase Supply

The circuit in Figure 3 uses multiple LT1506s to produce a 5V, 12A power supply. There are several advantages to using a multiple switcher approach compared to a single larger switcher. The inductor size is considerably reduced. Inductor size is proportional

to the energy that needs to be stored in the core. Three 4A inductors store less energy ($1/2Li^2$) than a single 12A coil, so they are much smaller. In addition, synchronizing three converters 120° out of phase with each other reduces input and output ripple currents. This reduces the ripple rating, size and cost of the filter capacitors.

Current Sharing/ Split Input Supplies

Current sharing is accomplished by connecting the V_C pins to a common compensation capacitor. The output of the error amplifier is a g_m stage, so any number of devices can be connected together. The effective g_m of the composite error amplifier is the product of the individual devices. In Figure 3, the compensation capacitor, C4, has been increased by 3x. Tolerances in the reference voltages cause small offset currents to flow between the V_C pins. The overall effect is that the loop regulates the output at a voltage somewhere between the minimum and maximum references of the devices used. Switch-current matching between devices will be typically better than 300mA over the full current range. The negative temperature coefficient of the V_C -to-switch-current transconductance prevents current hogging.

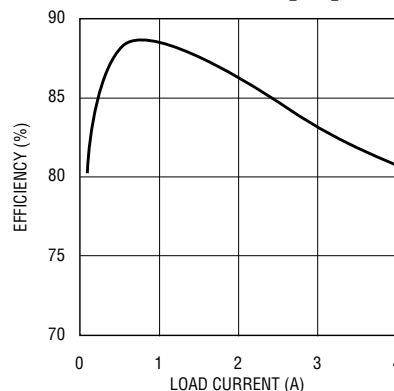


Figure 2. Efficiency vs load current for Figure 1's circuit

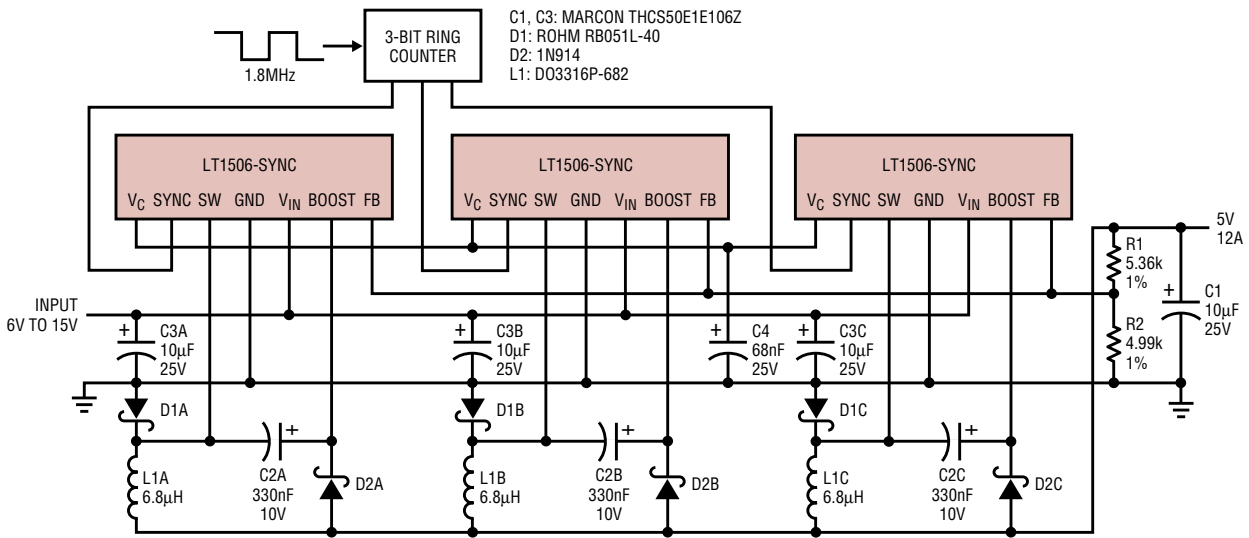


Figure 3. Current-sharing 5V/12A supply

A common V_C voltage forces each LT1506 to operate at the same switch current, not at the same duty cycle. Each device operates at the duty cycle defined by its input voltage. This is a useful feature in a distributed power system. The input voltage to each device could vary due to drops across

the backplane, copper losses, connectors and so on. The common V_C signal ensures that loading is still shared between the devices.

Synchronized Ripple Currents

A ring counter generates three synchronization signals at 600kHz, 33% duty cycle, phased 120° apart. The sync input will operate over a wide range of duty cycles, so no further pulse conditioning is needed. At full load, each device's input ripple current is a 4A trapezoidal wave at 600kHz, as shown in Figure 4. Summing these waveforms gives the effective input ripple for the complete system. The resultant waveform, shown at the bottom of Figure 4, remains at 4A but its frequency has increased to 1.8MHz. The higher frequency eases the requirements on the value of input filter without the $3\times$ increase in ripple current rating that would normally occur. Although only a single input capacitor is required, practical layout restrictions usually dictate an individual capacitor at each device. Figure 5 shows the output ripple current waveforms. The resultant 1.8MHz triangular waveform has a maximum amplitude of 350mA at an input voltage of 10V. This is significantly lower than would be expected for a 12A output. Interestingly, at inputs of 7.6V and 15V, the

theoretical summed output ripple current cancels completely. To reduce board space and ripple voltage, C1 and C3 are ceramic capacitors. Loop compensation capacitor C4 must be adjusted when using ceramic output capacitors, due to the lack of effective series resistance (ESR). The typical

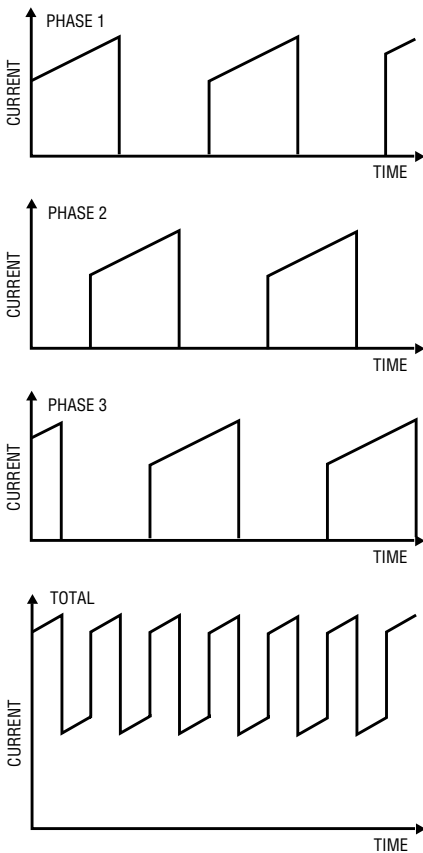


Figure 4. Input current

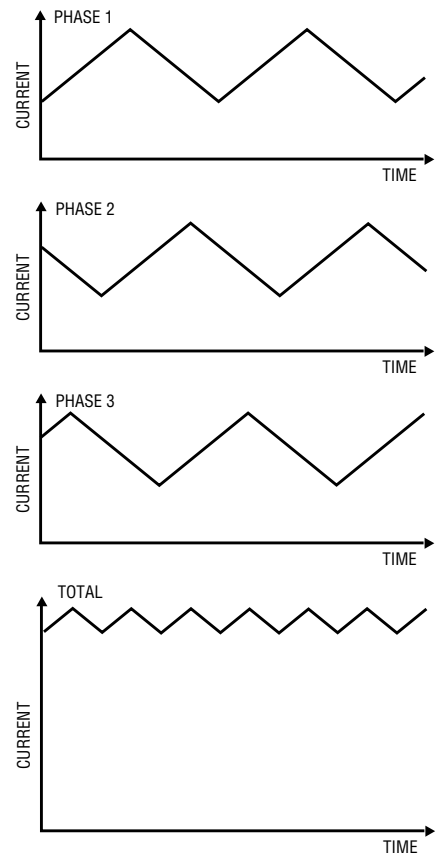


Figure 5. Output current

tantalum compensation value of 1.5nF is increased to 22nF (x3) for the ceramic output capacitor. If synchronization is not used and the internal oscillators free run, the circuit will operate correctly, but ripple cancellation will not occur. Input and output capacitors must be ripple rated for the individual output currents.

Redundant Operation

The circuit shown in Figure 3 is fault tolerant when operating at less than 8A of output current. If one power stage fails open circuit, the output will remain in regulation. The feedback loop will compensate by raising the voltage on the V_C pin, increasing the switch current of the two remaining devices.

5V to 3.3V at 2.5A on 0.25in² of board space, 0.125in High

In many space-sensitive applications, the component that dominates both board area and overall height is the inductor. One of the factors affecting inductor value choice is maximum ripple current. Using the high current switch rating of the LT1506,

higher ripple current can be tolerated, allowing the use of small, low value, high current inductors. A ceramic output capacitor also reduces board area and improves voltage ripple. Using Figure 1's circuit with the SO-8 LT1506 and the component changes in Table 1, a very small, low profile, step-down converter can be implemented.

Table 1. Component changes for a low profile version of Figure 1's circuit

Part	Value	Vendor/Part#
C1, C3	22µF, 10V	Tokin 1210ZG226Z
C _c	22nF	
L1	2.2µH	Sumida CD43 2R2

Conclusion

The LT1506 is a compact, easy to use, monolithic switcher. The internal 4.5A switch covers a wide range of medium power applications. Its input operating range of 4V to 15V and availability in SO-8 or DD packages make it ideal for very space-efficient, local onboard DC/DC converters. **LT**

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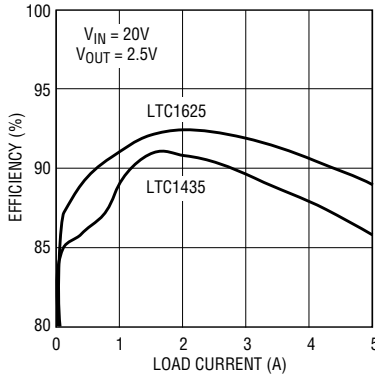
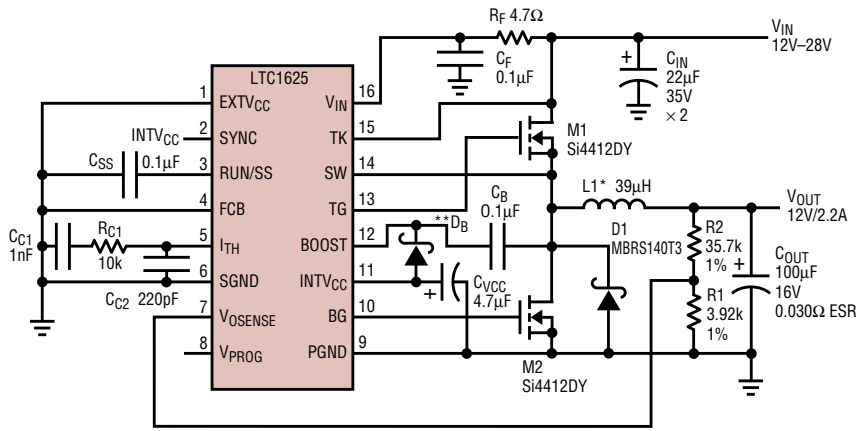


Figure 4. Efficiency vs load current



*L1 = SUMIDA CDRH127-390MC
 **D_B = CMDSH-3

Figure 5. 12V/2.2A adjustable-output supply

LTC1625, continued from page 4

A circuit demonstrating the wide output range of the LTC1625 is shown in Figure 5. This application uses Si4412DY MOSFETs to deliver a 12V output at up to 2.2A. Note that the SYNC pin is tied high for 225kHz operation in order to reduce the inductor size and ripple current.

Conclusion

The LTC1625 step-down DC/DC controller offers true current mode control without the expense and difficulty of using a sense resistor. Popular features from Linear Technology's other controllers, such as fixed frequency operation, N-channel MOSFET drive, Burst Mode operation, soft-start and output voltage programming make

this controller useful in a variety of applications. By eliminating the power loss in the sense resistor, even higher efficiencies can be achieved than were previously possible, making the LTC1625 an excellent choice for DC/DC converter designs requiring the highest performance. **LT**

48 Volt Hot Swap Controller for Negative Voltages

by Henry Yun
and Robert Reay

Introduction

As supply voltages for PC boards continue to drop, designers face the difficult task of minimizing the voltage drops through distributed power systems. At operating voltages of 3.3V or lower, the voltage drops across power busses, connector pins and inrush control circuitry can cause a supply voltage to drop out of tolerance. A solution to this problem is to distribute power at a high voltage, commonly 48V, and then step the voltage down to the final desired value on each board in the system, using power modules.

Most 48V power modules require an input bypass capacitor with a typical value of hundreds of microfarads. When the board is hot-plugged into a live 48V power rail, the input capacitor can draw huge inrush currents as it charges. The inrush current can cause permanent damage to the board's components and create glitches on the system power supply that can make the system function improperly.

The LTC1640H and LTC1640L provide a simple, flexible solution to -48V hot-swapping problems. The chips allow a board to be safely inserted into or removed from a live backplane with a supply voltage from -10V to -80V. They feature programmable inrush current control, programmable undervoltage and overvoltage protec-

tion, a programmable electronic circuit breaker and direct power-module-enable control.

Power Supply Control

A typical LT1640 application is shown in Figure 1. The input voltage of the power module on a circuit board is controlled by gradually increasing the gate voltage of the external N-channel pass MOSFET (Q1) in the power path. R1 provides current fault detection and R2 prevents high frequency oscillation. Resistors R4, R5 and R6 provide undervoltage and overvoltage sensing. Resistor R3 and capacitor C2 act as a feedback network to accurately control the inrush current. The waveforms are shown in Figure 2. The inrush current can be calculated with the following equation:

$$I_{\text{INRUSH}} = (45\mu\text{A} \times C_L) / C_2$$

where C_L is the total load capacitance.

Resistor R3 helps keep Q1 off when the power pins first make contact. When the power pins make contact, they bounce several times. While the contacts are bouncing, the LT1640 senses an undervoltage condition and the GATE is immediately pulled low.

Once the power pins stop bouncing, the GATE pin starts increasing until when Q1 turns on and the GATE voltage is held constant by the feedback network of R3 and C2. When the

DRAIN voltage has finished increasing, the voltage on the GATE pin then rises to its final value.

Electronic Circuit Breaker

The LT1640 features an electronic circuit-breaker function that protects against short circuits or excessive supply currents. By placing a sense

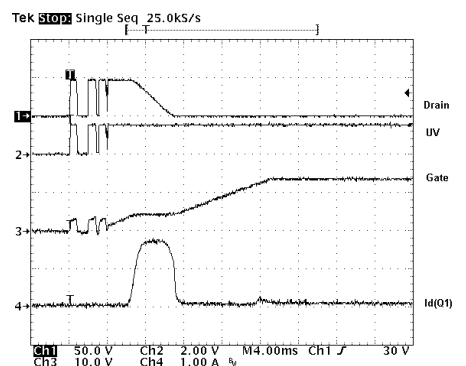


Figure 2. Inrush-current control waveforms

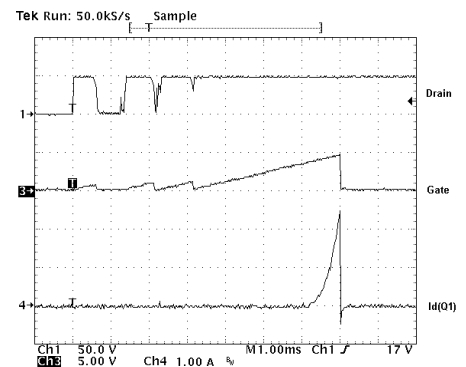


Figure 3. Short-circuit protection waveforms

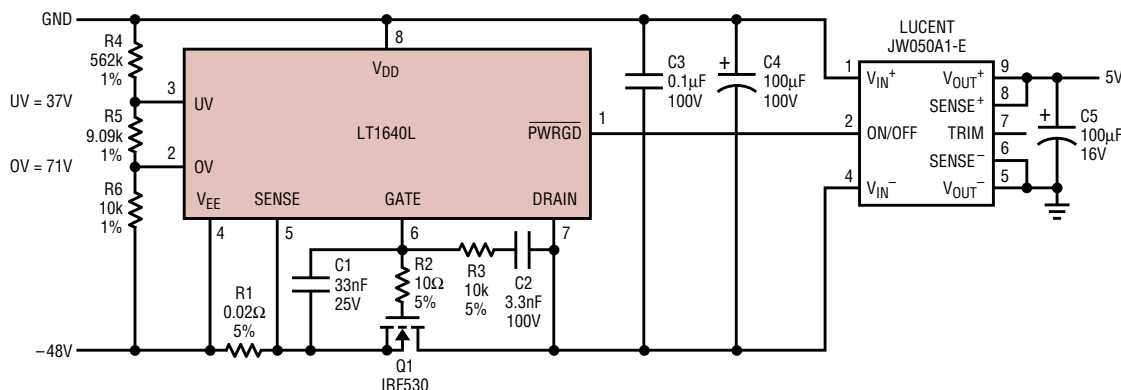


Figure 1. Typical LT1640 application with a power module

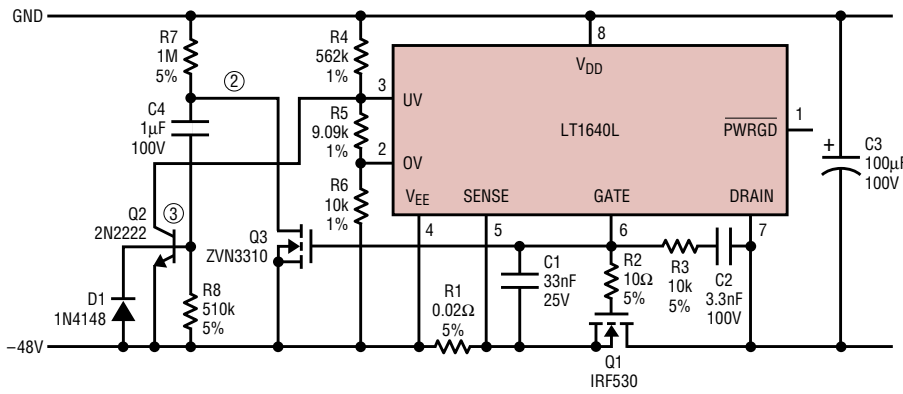


Figure 4a. This circuit resets the circuit breaker after a current fault.

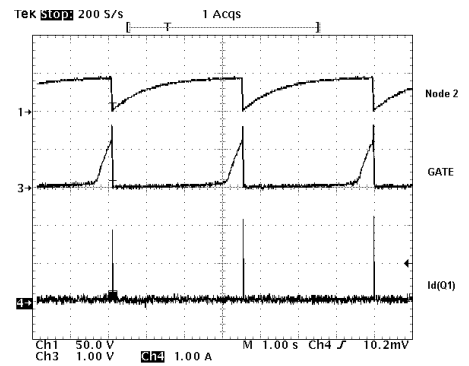


Figure 4b. Waveforms of Figure 4a's circuit

resistor between the V_{EE} and SENSE pins, the circuit breaker will be tripped whenever the voltage across the sense resistor is greater than 50mV for more than 3µs, as shown in Figure 3.

When the circuit breaker trips, the GATE pin is immediately pulled to V_{EE} and the external N-channel MOSFET is turned off. The GATE pin will remain low until the circuit breaker is reset by pulling UV low then high or cycling power to the part. A circuit that automatically resets the circuit breaker after a current fault is shown in figure 4.

Transistors Q2 and Q3, along with R7, R8, C4 and D1, form a programmable one-shot circuit. Before a short occurs, the GATE pin is pulled high and Q3 is turned on, pulling node 2 to V_{EE}. Resistor R8 turns off Q2. When a short occurs, the GATE pin is pulled low and Q3 turns off. Node 2 starts to charge C4, and Q2 turns on, pulling the UV pin low and resetting the circuit breaker. As soon as C4 is fully

charged, R8 turns off Q2, UV goes high and the voltage on the GATE starts to increase. Q3 turns back on and quickly pulls node 2 back to V_{EE}. Diode D1 clamps node 3 one diode drop below V_{EE}. The duty cycle is set to 10% to prevent Q1 from overheating.

Undervoltage and Overvoltage Detection

The UV (3) and OV (2) pins can be used to detect undervoltage and overvoltage conditions at the power supply input. The UV and OV pins are internally connected to analog comparators with 20mV of hysteresis. When the UV pin falls below its threshold or the OV pin rises above its threshold, the GATE pin is immediately pulled low. The GATE pin will be held low until UV is high and OV is low.

The undervoltage and overvoltage trip voltages can be programmed using a 3-resistor-divider, as shown in Figure 5.

With R4 = 562k, R5 = 9.09k and R6 = 10k, the undervoltage threshold is set to 37V and the overvoltage threshold is set to 71V.

PWRGD/PWRGD Output

The PWRGD/PWRGD output can be used to directly enable a power module when the input voltage to the module is within tolerance. The LT1640H has a PWRGD output for modules with an active-high enable input, and the LT1640L has a PWRGD output for modules with an active-low enable input.

When the DRAIN pin of the LT1640H is more than V_{PG} (1.4V) above V_{EE} (see Figure 6), internal transistor Q3 is turned off and R7 and Q2 clamp the PWRGD pin one diode drop (~0.7V) above the DRAIN pin. Transistor Q2 sinks the module's pull-up current and the module turns off.

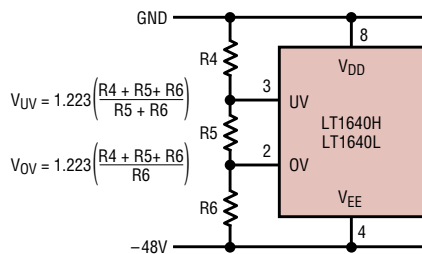


Figure 5. Undervoltage and overvoltage sensing

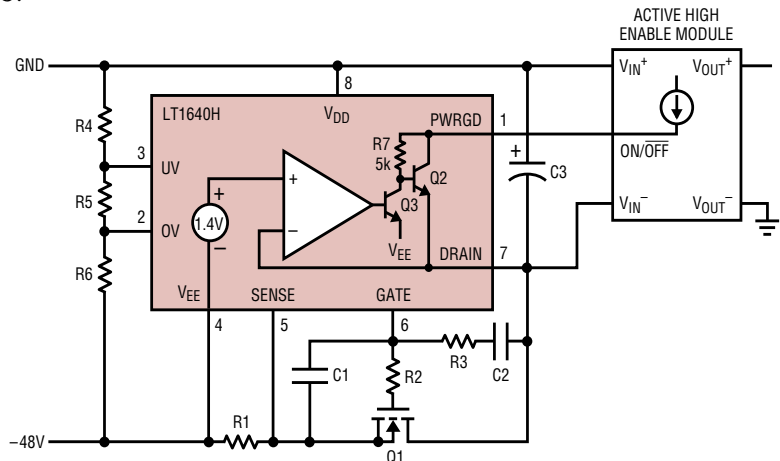


Figure 6. Active-high enable module

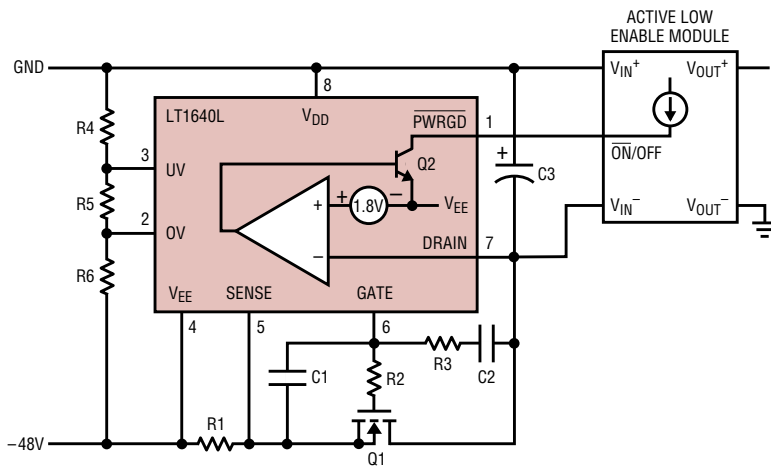



Figure 7. Active-low enable module

the GATE voltage will be about 2V below the supply voltage. At the minimum 10V supply voltage, the gate voltage is guaranteed to be greater than 6V and no greater than 18V for supply voltages up to 80V.

Conclusion

LT1640 provides a simple and flexible solution for hot swap applications. It is the first part that allows system designers to connect an 80V supply directly to the chip without any voltage step-down circuitry. It can be programmed to control the output slew up rate and the inrush current. It has programmable under-voltage and overvoltage protection, and the PWRGD/PWRGD output can be tied directly to a power-module enable pin. The LT1640 simplifies the design of high voltage hot-swap control systems and combines all of these features in an 8-pin SO/PDIP package. 

When the DRAIN pin drops below V_{PG} , Q3 will turn on, shorting the bottom of R7 to V_{EE} and turning Q2 off. The pull-up current in the module then flows through the R7, pulling the PWRGD pin high and enabling the module.

When the DRAIN pin of the LT1640 is more than V_{PG} (1.4V) above V_{EE} , the internal pull-down transistor, Q2, is off and the PWRGD pin is in high impedance state (see Figure 7). The PWRGD pin will be pulled high by the module's internal pull-up current source, turning the module off. When the DRAIN pin drops below V_{PG} , Q2 will turn on, and the PWRGD pin will be pulled low, enabling the module.

The PWRGD signal can also be used to turn on an LED or optoisolator to indicate that the power is good, as shown in Figure 8.

Gate Pin Voltage Regulation

When the supply voltage to the chip is more than 15.5V, the GATE pin voltage is regulated at 13.5V above V_{EE} . If the supply voltage is less than 15.5V,

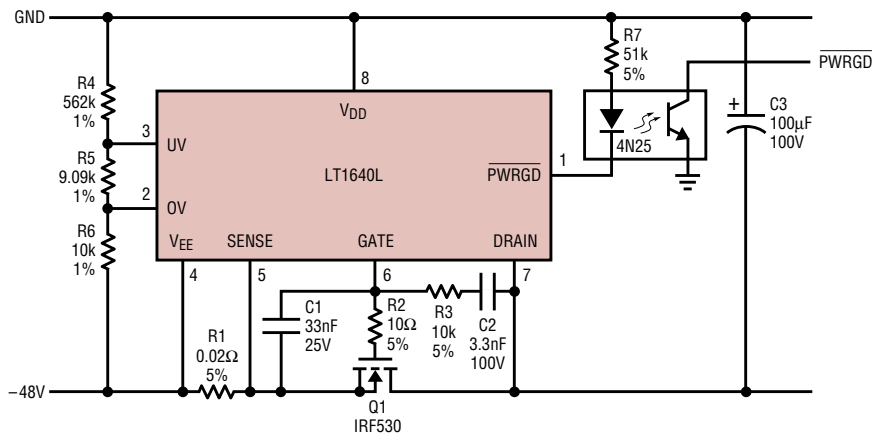


Figure 8. Using PWRGD to drive an optoisolator

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Hot Swapping the PCI Bus Using the LTC1643

by Robert Reay

Hot Circuit Insertion

When a circuit board is inserted into a live PCI slot, the supply bypass capacitors on the board can draw huge transient currents from the PCI power bus as they charge. The transient currents can cause permanent damage to the connector pins and create glitches on the power bus, causing other boards in the system to reset.

The LTC1643 is designed to turn a board's supply voltages on and off in a controlled manner, allowing the board to be safely inserted into or removed from a live PCI slot without causing glitches on the system power supplies. The chip also protects the PCI supplies from short circuits and monitors the supply voltages.

The LTC1643H is designed for motherboard applications, whereas the LTC1643L is designed for CompactPCI applications where the chip resides on the plug-in board. The part is available in the space saving 16-pin SSOP package.

LTC1643 Features

- Allows safe insertion into and removal from either a motherboard (LTC1643H) or CompactPCI board (LTC1643L)
- Controls all four PCI supplies: -12V, 12V, 3.3V and 5.0V
- Programmable foldback current limit: a programmable analog current limit with a value that depends on the output voltage. If the output is shorted to ground, the current limit drops to keep power dissipation and supply glitches to a minimum.
- Programmable circuit breaker: if a supply remains in current limit too long, the circuit breaker will trip, the supplies will be turned off and the FAULT pin will be pulled low.
- Current-limit power up: the supplies are allowed to power up in current limit. This allows the chip to power-up boards with widely varying capacitive loads without tripping the circuit breaker. The maximum allowable power-up time is programmable using the TIMER pin.

- 12V and -12V power switches on-chip
- Power-good output: monitors the voltage status of the four supply voltages.

PCI Power Requirements

All PCI connectors require four power rails: 5V, 3.3V, 12V and -12V. Systems implementing the 3.3V signaling environment are always required to provide all four rails in every system. Systems implementing the 5V signaling environment may either ship the 3.3V supply with the system or provide a means to add it afterward. The tolerance of the supplies as measured at the plug-in card is summarized in Table 1.

Table 1. PCI power supply requirements

Power Rail	Current	Typical Capacitance
5V $\pm 5\%$	5A	<3000 μ F
3.3V $\pm 0.3V$	7.5A	<3000 μ F
12V $\pm 5\%$	500mA	<330 μ F
-12V $\pm 10\%$	100mA	<120 μ F

Power-Up Sequence

The power supplies are controlled by external N-channel pass transistors Q1 and Q2 in the 3.3V and 5.0V power paths and internal pass transistors for the 12V and -12V power paths (see Figure 1).

Resistors R1 and R2 provide current-fault detection and R7 and C1 provide current-control loop compensation. Resistors R5 and R6 prevent high frequency oscillations in Q1 and Q2.

When the ON pin (5) is pulled high, the pass transistors are allowed to turn on and a 20 μ A current source is connected to the TIMER pin (4) (see Figure 2). The current in each pass transistor increases until it reaches the current limit for each supply.

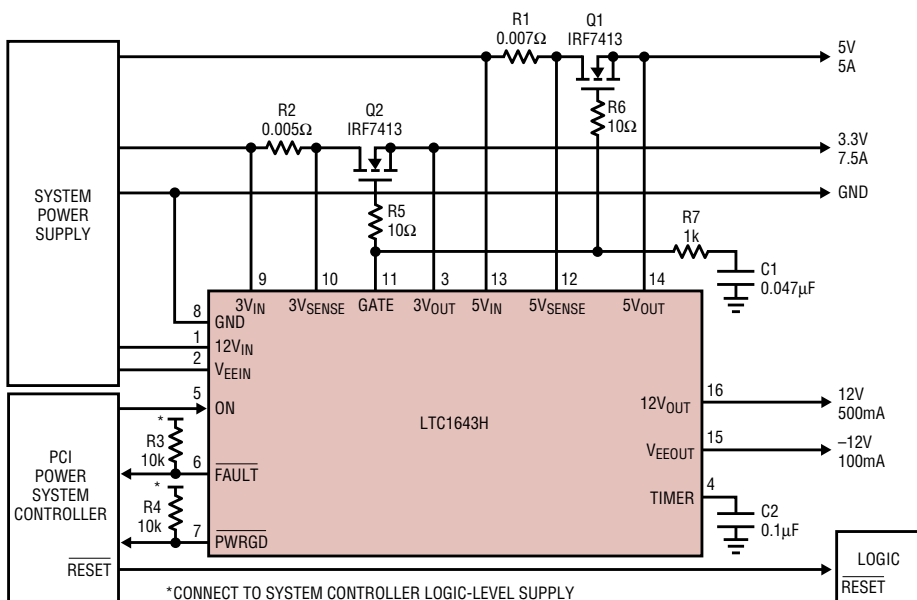


Figure 1. Typical LTC1643H application

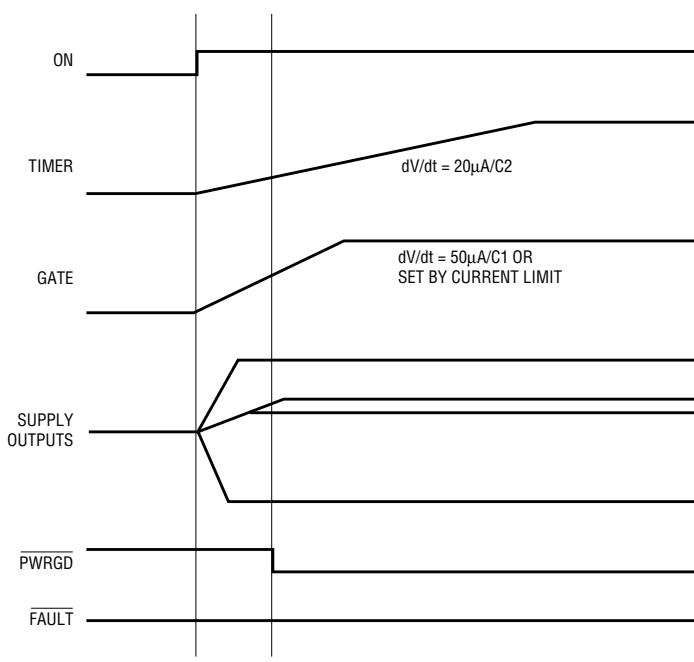


Figure 2. Normal power-up sequence

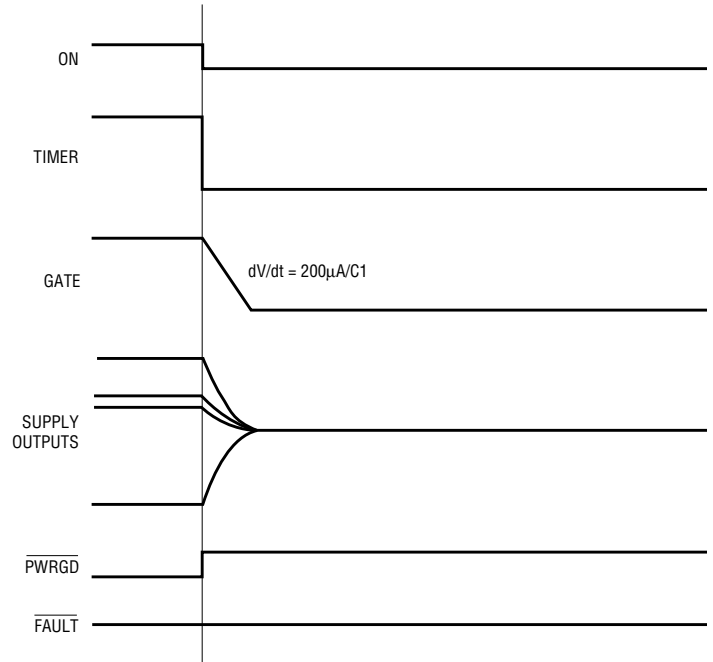


Figure 3. Normal power-down sequence

Power-Down Sequence

Each supply is then allowed to power up at a rate controlled either by the current limit into the load capacitance or $dv/dt = 50\mu A/C1$, whichever is slower. Current limit faults are ignored until the voltage on the TIMER pin (4) reaches 1V below the $12V_{IN}$ pin (1). Once all four supply voltages are within tolerance, the PWRGD pin (7) will be pulled low.

When the ON pin (5) is pulled low, a power-down sequence begins (see Figure 3). Internal switches are connected to each of the output supply voltage pins to discharge the bypass capacitors to ground. The TIMER pin (4) is immediately pulled low. The voltage on the GATE pin (11) is discharged by a $200\mu A$ current source to prevent the load currents on the 3.3V and 5.0V supplies from going to zero

instantaneously and causing glitches on the power supplies. When any of the output voltages dips below its threshold, the PWRGD pin (7) is pulled high.

Timer

During a power-up sequence, a $20\mu A$ current source is connected to the TIMER pin (4) and current limit faults are ignored until the voltage on this pin increases to within 1V of the $12V_{IN}$ pin (1). This feature allows the chip to power-up PCI cards with widely varying capacitive loads on the supplies. The power-up time will be:

$$t_{ON} = 2 \times (C_{SUPPLY} \times V_{SUPPLY}) / (I_{LIMIT} - I_{LOAD})$$

For $C_{SUPPLY} = 2000\mu F$, $V_{SUPPLY} = 5V$, $I_{LIMIT} = 7A$, $I_{LOAD} = 5A$ the turn on time will be $\sim 10ms$. The timer period should be set longer than the maximum supply turn-on time but short enough to not exceed the maximum safe operating area of the pass transistor during a short circuit. The TIMER period will be:

$$t_{TIMER} = (C_{TIMER} \times 11.1V) / 22\mu A$$

For $C_{TIMER} = 0.1\mu F$, the TIMER period will be $\sim 50ms$. The TIMER pin

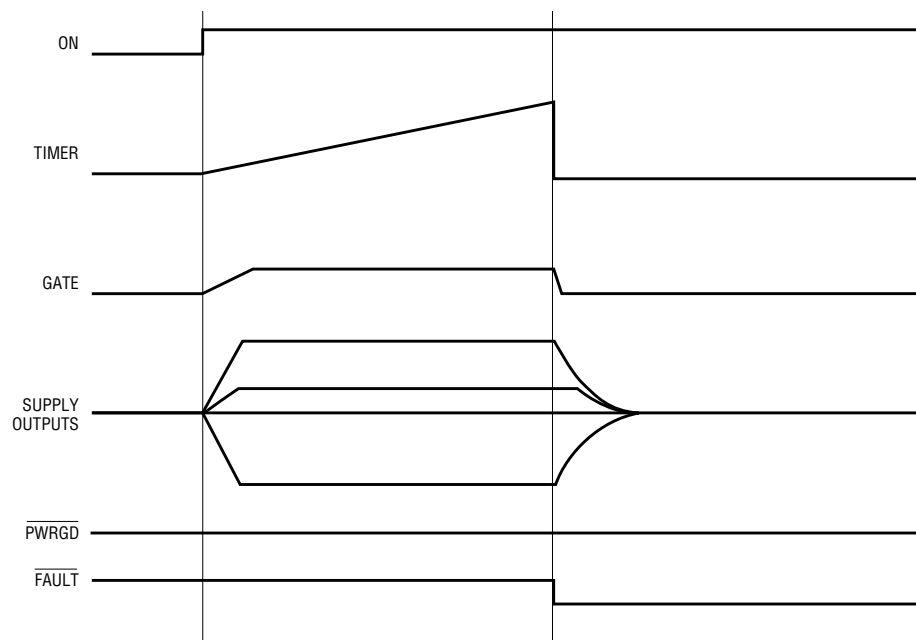


Figure 4. Power-up into a short circuit on a 3.3V output

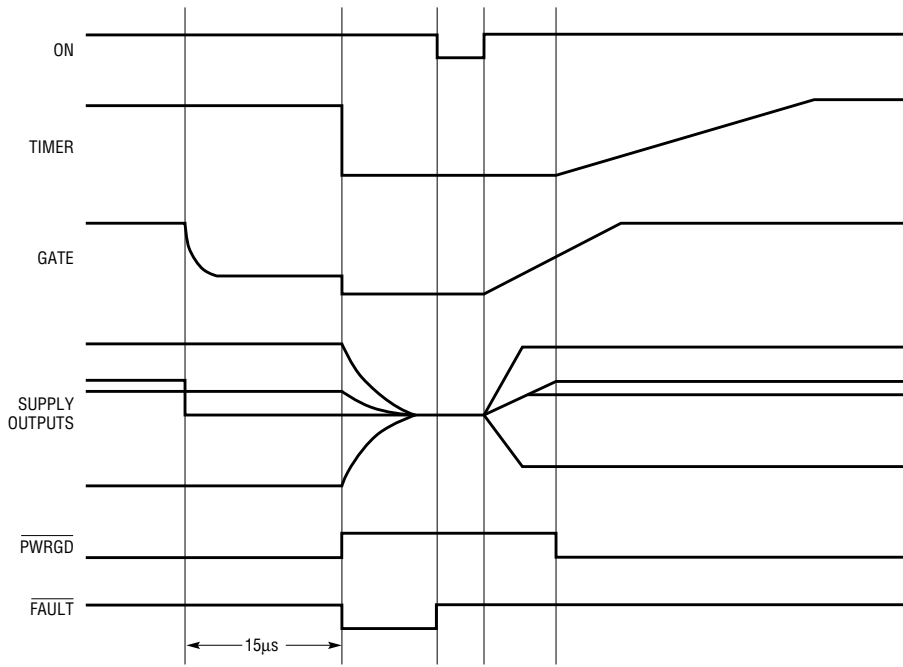


Figure 5. Short circuit on 5V

(4) is immediately pulled low when the ON pin (5) goes low.

Thermal Shutdown

The internal switches for the 12V and -12V supplies are protected by an internal current limit and thermal shutdown circuit. When the temperature of the chip reaches 150°C, all switches will be latched off and the FAULT pin (6) will be pulled low.

Short-Circuit Protection

During a normal power-up sequence, if the voltage on the TIMER pin (4) has reached its maximum and a supply is still in current limit, all of the pass transistors will be immediately turned off and the voltage on the FAULT pin (6) will be a logic low, as shown in Figure 4. If a short circuit occurs after the supplies are powered-up, the shorted supply's current will drop immediately to the limit value (see Figure 5).

If the supply remains in current limit for more than 15µs, all of the supplies will be latched off. The 15µs delay prevents quick current spikes, for example from a fan turning on, from causing false trips of the circuit breaker. The chip will stay in the latched-off state until the ON pin (5)

is cycled low then high or the 12V_{IN} power supply is cycled.

To prevent excessive power dissipation in the pass transistors and prevent voltage spikes on the supplies during short-circuit conditions, the current limit on each supply is designed to be a function of the output voltage. As the output voltage drops, the current limit decreases. Unlike a traditional circuit breaker function, where huge currents can flow before the breaker trips, the cur-

rent foldback feature ensures that the supply current will be kept at a safe level and prevent voltage glitches while applying power into a short.

The current limit for the 5.0V and 3.3V supplies is set by placing a sense resistor between 5V_{IN} (pin 13) and 5V_{SENSE} (pin 12) and between 3V_{IN} (pin 9) and 3V_{SENSE} (pin 10). The current limit will be set by:

$$I_{LIMIT} = 53mV/R_{SENSE}$$

For a 0.005Ω resistor, the current limit will be set at 10.6A and foldback will be set to 1.5A when the output is shorted. For a 0.007Ω resistor, the current limit will be set at 7.6A and foldback to 1.1A when the output is shorted. The current for the internal 12V switch is set at 1A, folding back to 300mA, and that for the -12V switch is set at 450mA, folding back to 150mA.

A CompactPCI Application

CompactPCI is an open standard for a hot swappable industrial PCI bus supported by the PCI Industrial Manufacturer's Group. The CompactPCI specification calls for the power control to be located on the plug-in board rather than the backplane. The typical application is shown in Figure 6. Because the turn-on signal is active low for CompactPCI, the LTC1643L must be used.

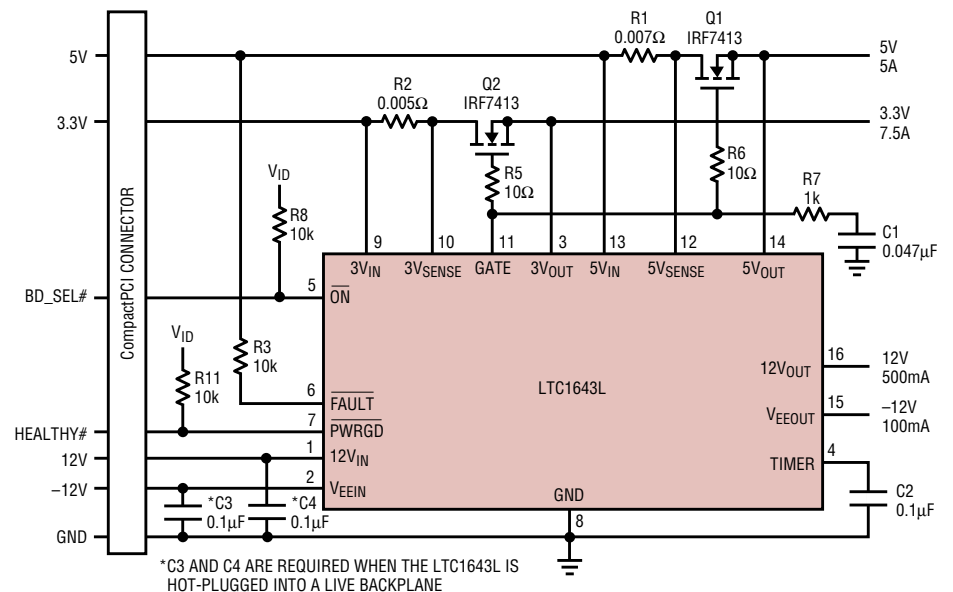


Figure 6. Typical CompactPCI application

Eliminate Pipeline Headaches with New 12-Bit 3MSPS SAR ADC

by Dave Thomas and William C. Rempfer

A new 12-bit 3MSPS ADC brings new levels of performance and ease of use to high speed ADC applications. By raising the speed of the successive approximation (SAR) method to 3MSPS, it eliminates the many drawbacks of pipelined and subranging ADCs in that speed range. It is the first clean, simple to use alternative to pipelined ADCs for applications up to 3MSPS.

The LTC1412 is an ultrafast SAR ADC that offers an ideal combination of performance, size and cost. Some of its features include:

- ❑ Complete low power 12-Bit 3MSPS ADC
- ❑ Great AC performance: 72.2dB SINAD and -80dB THD at Nyquist
- ❑ Great DC performance: $\pm 0.25\text{LSB}$ typical INL and DNL ($\pm 1\text{LSB}$ max)
- ❑ Three-state output bus with no pipeline delay (parallel I/O with DSP interface signals)
- ❑ Tiny SSOP-28 package

Drawbacks of Pipelined ADCs

Pipelined ADCs are great for what they do: giving the fastest speed short of using a full-flash converter. In fact, LTC manufactures both pipelined and subranging ADCs. However, these architectures do have a number of fundamental drawbacks that can cause headaches for the user. If they can be avoided, they should be. Until now, there was no alternative for 12-bit converters faster than 1.25MSPS. Now there is: the LTC1412. It does everything a pipelined ADC does, but doesn't have the drawbacks.

We will look at a number of headaches experienced by users of pipelined ADCs and then look at how the new SAR ADC can eliminate them.

Headache #1: Unpredictable Behavior

Because pipelined ADCs are more complex, they have more things to go wrong and often are more prone to temperamental behavior. First, because they contain flash ADCs, they can be susceptible to sparkle code problems that historically have occurred in flash ADCs. Also, because they contain multiple flash ADCs that are pieced together with sample-and-holds, errors can occur during the piecing together process at the points where they are joined. Often, these devices include correction circuitry to try to correct any errors that occur, but errors may change with reference voltage, temperature, supply voltage or other conditions and exceed the correction range. Behavior may change and errors result as reference voltage is varied, for instance.

Headache #2: Poor Noise and SNR

Because pipelined ADCs have a series of stages, the signal is passed down many times before it reaches the end

of the pipe. In addition to the errors described above, each pass will introduce noise into the signal and degrade the SNR and noise of the converter. SNR numbers for 12-bit pipelined ADCs range as low as 64dB typical (only 10.3 effective bits). Even the best SNR is only 70dB typical (11.3 effective bits). That is several dB (or one-half of a bit) below what is possible with a good SAR ADC (see Figure 1).

Headache #3: Poor Linearity

Pipelined ADCs are often resistor-string based and therefore suffer from INL problems that result from nonlinearities in the resistor string. These nonlinearities are impossible to trim or correct for, so they remain to degrade linearity. Linearity errors reported for these ADCs can be as bad as 4LSBs.

Headache #4: Complex Reference Circuitry and Weird Biasing Schemes

Pipelined ADCs usually require multiple reference pins for their internal flash ladders. They often require weird biasing schemes for driving the top and bottom of the reference ladder. Extra hardware is often required to provide low impedances to the multiple reference pins. On some converters, fast buffer amps are required; others require multiple bypass caps (see Figure 2).

In addition to the extra hardware to generate the multiple reference voltages, the ADC range is no longer controlled by a single reference voltage. This means that more complicated circuitry may be required to change the ADC's full scale range.

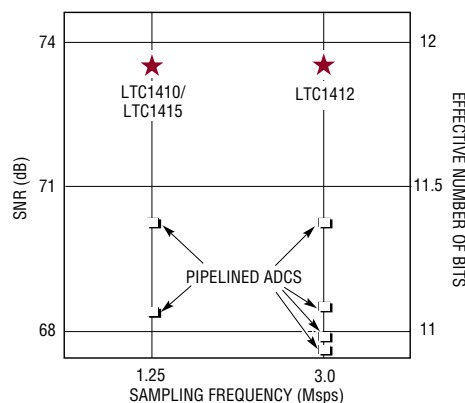


Figure 1. Because the input signal to a pipelined ADC passes from stage to stage and is resampled each time, the noise will not be as good as in a SAR ADC where the signal is sampled once and then converted. A collection of pipelined ADCs shows inferior SNR to the new 3MSPS LTC1412.

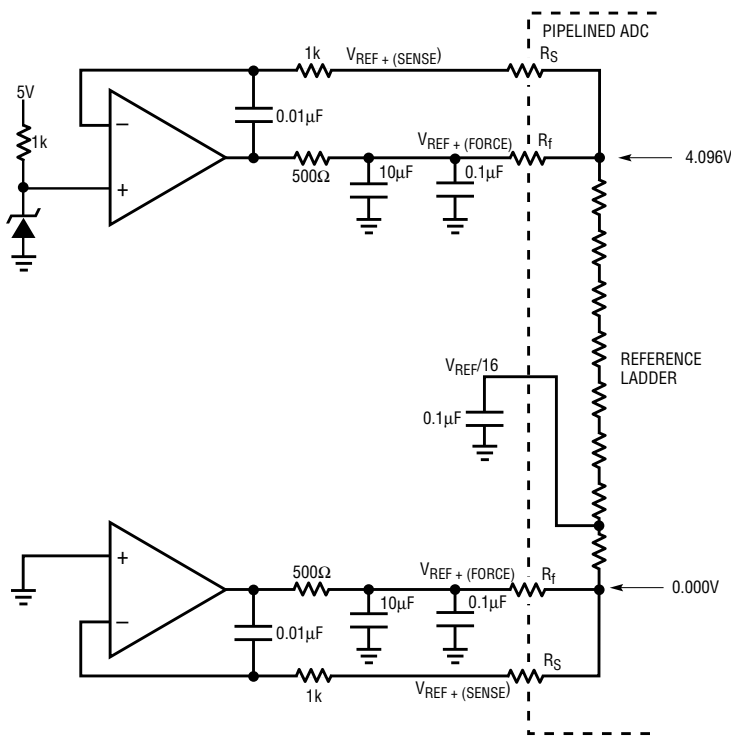


Figure 2. Multiple reference pins are required for the top and bottom of the internal flash ladders on most pipelined ADCs. Extra hardware is required to provide low impedance to the reference pins. In addition, input scaling can not be accomplished by varying a single reference voltage.

**Headache #5:
Complicated Input Circuitry**

Another complication with pipelined ADCs is the input circuitry. Some of these ADCs require complementary differential input signals to perform correctly. Two signals 180° out of phase must be applied. Further, the signals must have an accurate common mode voltage. This means that complicated level shifting circuitry must be used to manipulate the signal into a form suitable for the ADC (see Figure 3a). Transformers are often required to get good performance from the ADC, as shown on the product data sheets (see Figure 3b).

Headache #6: Pipeline Delay

Pipeline converters have pipeline delay, which is a latency between the input sample and the corresponding data at the ADC output. Latencies can be as high as seven clock cycles. This latency can ruin the device's usefulness in many types of applications, including high speed servo-loop control systems, motor control, asynchronous or event driven sampling,

multiplexing systems and others that require a one-to-one time correspondence between each sample and the corresponding data.

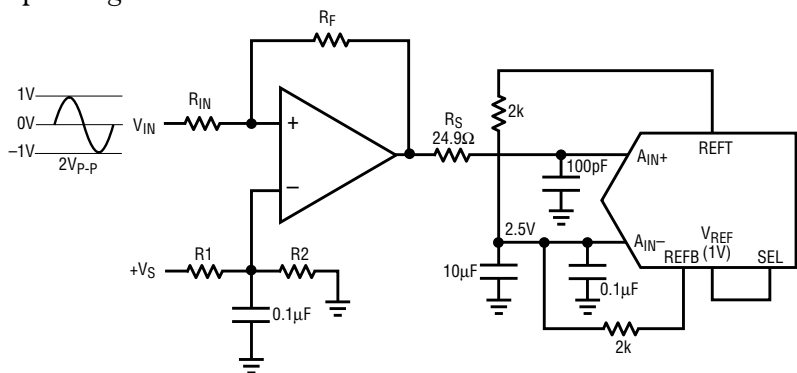


Figure 3a. Example of a pipelined ADC input-drive circuit

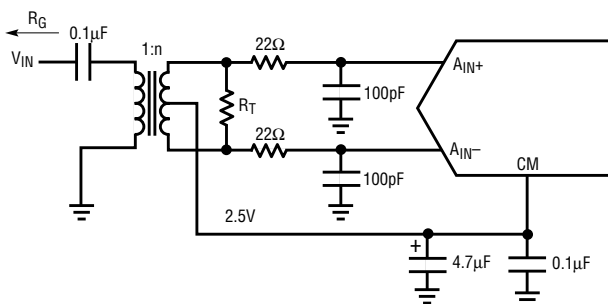


Figure 3b. Example of a transformer-coupled input-drive circuit for a pipelined ADC

In addition, these ADCs require continuous sampling and do not operate well when sampling stops and starts. When sampling stops, the internal sample-and-holds droop and samples in the pipeline are lost. Figure 8 shows how accuracy is lost as the sample rate is reduced. When conversions restart, the pipeline has to be flushed before accurate data can be received.

Moreover, many devices have dynamic internal biasing, which gets lost when the clock stops. In this case, even the biasing for the internal amplifiers is lost. This requires even more clock cycles to restore the bias in addition to those required to flush the pipeline.

**Headache #7:
No Three-State on Data Outputs**

Pipeline converters typically don't provide a way to disable the output bus. They can only be connected to a single DSP or receiving logic and cannot share a bus or have their outputs MUXed with those of other ADCs.

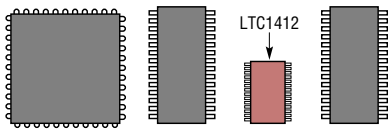


Figure 4. Package size is another disadvantage of pipelined ADCs. The more complex and much larger chips require much larger package sizes than high performance SAR devices.

Headache #8: Poor Frequency Domain Performance

Pipelined ADCs have a variety of problems that degrade frequency domain performance. First, because the signal passes from stage to stage and is resampled each time, the noise will not be as good as with a SAR ADC, where the signal is sampled once and then converted. As mentioned earlier, SNRs can be very poor for these ADCs. The best ones give up several dB (one-half bit) relative to a good SAR converter.

Some devices show terrible high frequency dynamic performance because the input signal is sampled at different times by the different parts of the internal circuitry. Because the delays of the internal circuits are not the same, the input signal is sampled at different times. Severe distortion results when high frequency signals are digitized by these devices.

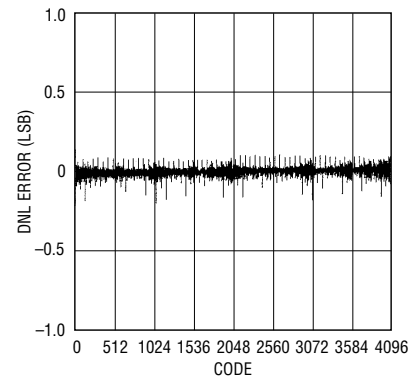
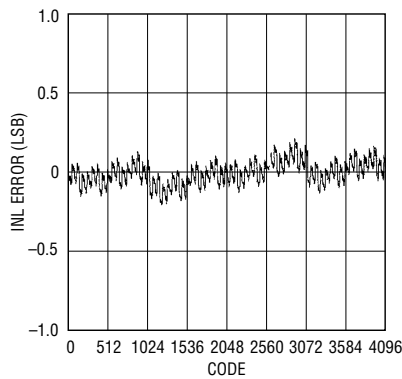


Figure 5. Because the LTC1412 depends solely on capacitor matching for accuracy (unlike pipelined ADCs), both its INL and DNL are typically 0.25LSB and do not drift with time, temperature, supply voltage or reference voltage. Maximum DNL and INL are both ± 1 LSB.

Headache #9: DC vs AC Performance Compromises

Some pipelined ADCs can't deliver good DC and AC performance at the same time. They require a low reference voltage and small input span to deliver good AC performance, but DC performance is unspecified and noise is poor. On the other hand, they require a large input span and high reference voltage to get good noise and specified DC performance, but the AC performance is poor under these conditions. In these devices, good AC and DC performance cannot be achieved simultaneously.

Headache #10: Large Package Size

Because they are complex and often have several large flash ADCs inside, the pipelined ADCs require larger package sizes than SAR converters. Package sizes range up to 44-lead PLCCs that are twice the size of the 28-lead SSOP of the LTC1412 (see Figure 4).

How Do You Spell Relief?... L-T-C-1-4-1-2

As we said, relief from pipeline headaches is now available for sample rates up to 3MSPs. The new LTC1412 eliminates many of the drawbacks, as we will now see.

Excellent Linearity

Because it is a capacitively-based SAR ADC, the LTC1412 exhibits outstanding linearity, both DNL and INL. Because it depends solely on capacitor matching for accuracy (and not on amplifier gain or interstage S/H errors), both its INL and DNL are typically 0.25LSB and have virtually zero drift with time, temperature, supply voltage or reference voltage. Maximum INL and DNL are both ± 1 LSB. Figure 5 shows the outstanding INL and DNL of the LTC1412.

Simple Reference Circuitry (1 Cap) and 1-Pin Gain Adjust

Figure 6 shows the hookup of the LTC1412. Because it is a SAR converter, a single reference voltage sets the full-scale range of the input. The range can be adjusted by driving the reference pin.

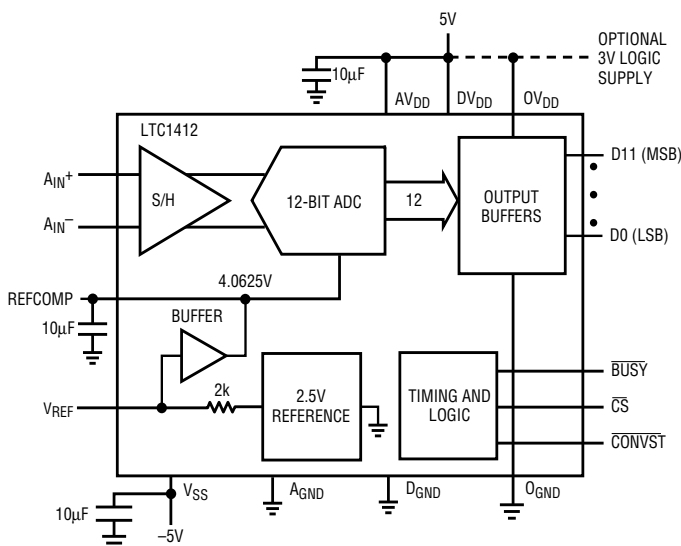


Figure 6. The hookup of the new SAR converter is simple. A single reference voltage (buffered to appear at the REFCOMP pin) controls the span of the ADC. The flexible differential input accepts differential or single-ended inputs equally well and operates without needing signal inversion circuitry or transformer coupling.

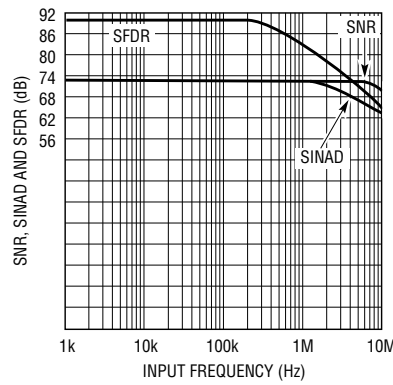
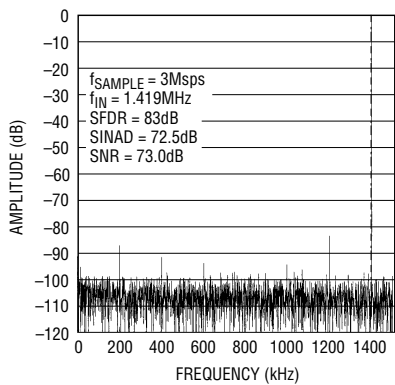


Figure 7. The LTC1412 has near perfect SNR, THD and SINAD even at the Nyquist input frequency of 1.5MHz. (a) shows SNR of 73dB. This, combined with the 80dB THD, gives a SINAD of 72.2dB at Nyquist. (b) shows how well the SNR, THD and SINAD hold up with high input frequencies.

For slow adjustments in the span, the REF pin can be driven and the internal buffer will generate the REFCOMP voltage used by the ADC. This is appropriate in communications applications where the gain is adjusted and remains stable for a time. If fast adjustments are required, the REFCOMP pin can be driven directly. In this case, the V_{REF} pin is tied to ground to disable the buffer. This works well for applications such as imaging, where a pixel-by-pixel correction in gain is required. The capacitive SAR architecture provides inherently good linearity over a 2:1 range of reference voltages.

Very Low Noise

The LTC1412 has nearly perfect noise performance. Because of its SAR architecture, its single S/H and its single-pass conversion, it adds almost no extra noise to the input signal. Its 73dB SNR (11.83ENOB) is within 1dB of the theoretical quantization noise for a 12-bit ADC (12 bits \times 6.02dB/bit + 1.76dB = 74dB theoretical). And its low aperture jitter (<5ps) maintains this nearly perfect SNR even with inputs up to the Nyquist frequency.

No other ADC comes close to this performance at 3Msps. It is at least 3dB (one-half of an effective bit) better than any other product and is 12dB (two bits) better than some (see Figure 1). Figure 7a shows an FFT of the LTC1412 at Nyquist. The noise floor corresponds to an SNR of 73dB.

Along with the very low noise, the LTC1412 also has premier distortion performance of 80dB at Nyquist (see Figure 7a). Combined with the 73dB SNR, this gives a SINAD at Nyquist of 72dB, a figure unmatched by any competing 12-bit device and better than most 14-bit devices. Figure 7b shows that the SNR, SINAD and THD remain excellent at high input frequencies.

Outstanding AC and DC Performance Simultaneously

The LTC1412 provides the near perfect AC performance mentioned above and outstanding linearity at the same time. Figures 5 and 7 were generated without having to change the input range or any other part of the configuration.

No Pipeline Delay—Start/Stop OK—Instant Start-Up

The LTC1412 has no pipeline delay. This means that when a conversion is started, the result of that conversion is ready 300ns later. This is in contrast to converters that can have seven cycles of delay (2.3 μ s at 3Msps) between the conversion start and the data.

Although some applications are not sensitive to this delay, many are. For example, in many event-driven sampling systems, as each event occurs, it is sampled and the resulting data is required before the next event occurs. In these cases, the LTC1412 can digitize and provide the

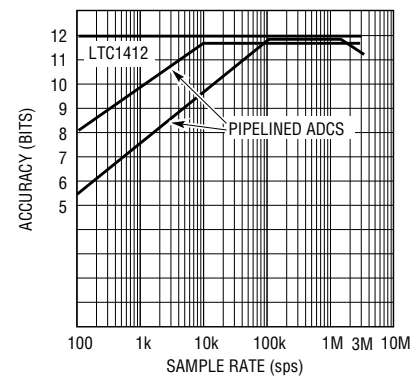


Figure 8. The zero pipeline delay of the LTC1412 makes it useful in time-domain applications such as high speed event driven sampling, DSP control loops and MUXed applications.

result in 300ns and be ready for the next sample. In contrast, a pipelined ADC would not work in these applications because its seven cycles of delay would require 2.3 μ s and create the problem of flushing the pipeline for each sample.

High speed control loops are another area where data latency is unacceptable (for loop stability). The LTC1412 can support a full 3Msps data rate with no latency. Examples of this type are motor control and high speed DSP servo-control loops.

The problems with MUXing pipelined converters are gone with the LTC1412. Its zero pipeline delay makes MUXing easy because it is easy to keep track of what sample is being converted.

Finally, because there is no minimum sample rate, starting and stopping the sample clock causes no problems for the converter. The first conversion after a long pause will be fully accurate, just like any other conversion (see Figure 8). This makes the LTC1412 perfect for data acquisition systems where sampling is asynchronous and the ADC must convert after a long inactive period, without any start-up time.

Clean, Simple, Well Behaved... No Erratic Behavior

The LTC1412 is a clean machine and is easy to lay out and implement. The SAR architecture is not susceptible to sparkle codes or other erratic be-

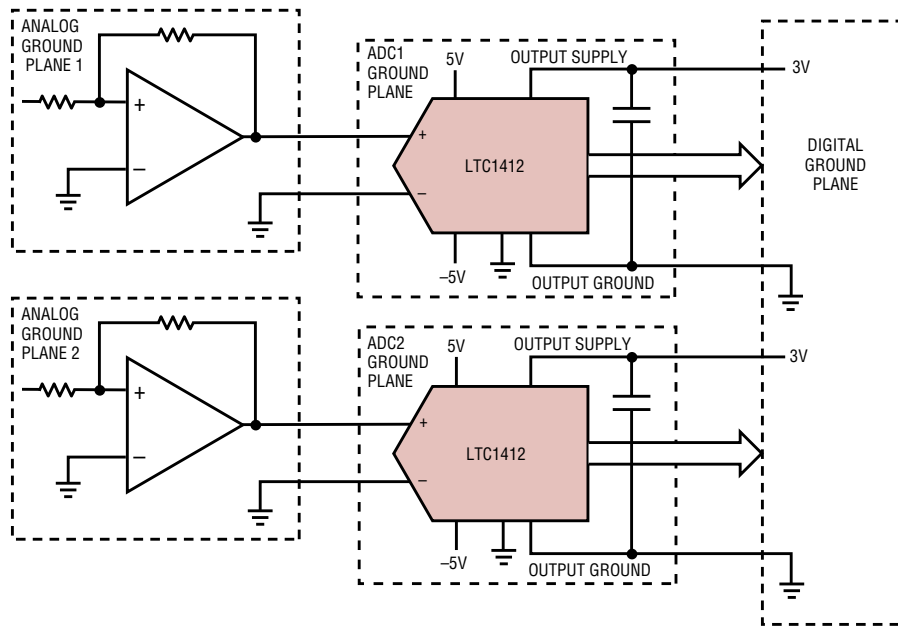


Figure 9. The LTC1412 simplifies grounding: differential inputs allow clean capture of signals, even from another board in the system. Output supply and ground allow multiple data converters to be combined at the logic section without creating system ground currents.

havior and performs very well, given reasonable care. Figure 6 shows a couple of nice features of the device. First, the differential inputs are great for eliminating noise. Routing them together on the board to the signal input will reject ground noise that may be present across the board. Second, the separate logic output supply and ground not only make for an easy interface to 3V, but simplify connections to the logic section as well.

Figure 9 shows how this can greatly simplify the grounding in large systems or multiple ADC systems. First,


the grounds in the vicinity of each ADC can be kept clean. Second, the differential inputs allow signals to be cleanly captured, even from another board in the system. Finally, the outputs of all the data converters can be combined at the logic section without generating ground currents throughout the system.

Efficient and Small Package

Because it is a simple, efficient architecture, the die size is small and the LTC1412 can fit in a tiny package. Instead of the very large packages used by pipelined parts, the LTC1412

comes in a tiny SSOP-28. A comparison to competitive pipelined parts is shown in Figure 4.

Conclusion

Pipelined ADCs are useful at very high sample rates but they do have drawbacks, as we have seen. Until now, designers had to use pipelined converters to get speeds up to 3MSPs, but no more. Now there is a clean SAR alternative: the LTC1412. It does everything a pipelined ADC does, but doesn't have the drawbacks. It is a sure cure for pipeline headaches. 



Component and Measurement Advances Ensure 16-Bit DAC Settling Time (Part One)

by Jim Williams

Introduction

Instrumentation, waveform generation, data acquisition, feedback control systems and other application areas are beginning to utilize 16-bit data converters. More specifically, 16-bit digital-to-analog converters (DACs) have seen increasing use. New components (see the sidebar “Components for 16-Bit Digital-to-Analog Conversion” on page 31) have made 16-bit DACs a practical design alternative. These ICs provide 16-bit performance at reasonable cost compared to previous modular and hybrid technologies. The DC and AC specifications of the monolithic DACs approach or equal previous converters at significantly lower cost.

DAC Settling Time

DAC DC specifications are relatively easy to verify. Measurement techniques are well understood, albeit often tedious. AC specifications require more sophisticated approaches to produce reliable information. In particular, the settling time of the DAC and its output amplifier is extraordinarily difficult to determine to 16-bit resolution. DAC settling time is the elapsed time from input code application until the output arrives at and

remains within a specified error band around the final value. It is usually specified for a full-scale 10V transition. Figure 1 shows that DAC settling time has three distinct components. The *delay time* is very small and is almost entirely due to propagation delay through the DAC and output amplifier. During this interval there is no output movement. During *slew time* the output amplifier moves at its highest possible speed towards the final value. *Ring time* defines the region where the amplifier recovers from slewing and ceases movement within some defined error band. There is normally a trade-off between slew and ring time. Fast-slewing amplifiers generally have extended ring times, complicating amplifier choice and frequency compensation. Additionally, the architecture of very fast amplifiers usually dictates trade-offs that degrade DC error terms.

Measuring anything at any speed to 16 bits ($\approx 0.0015\%$) is hard. Dynamic measurement to 16-bit resolution is particularly challenging. Reliable 16-bit settling-time measurement constitutes a high order difficulty problem requiring exceptional care in approach and experimental technique.

Considerations for Measuring DAC Settling Time

Historically, DAC settling time has been measured with circuits similar to that in Figure 2. The circuit uses the “false sum node” technique. The resistors and DAC-amplifier form a bridge-type network. Assuming ideal resistors, the amplifier output will step to V_{IN} when the DAC inputs move to all ones. During slew, the settle node is bounded by the diodes, limiting voltage excursion. When settling occurs, the oscilloscope probe voltage should be zero. Note that the resistor divider’s attenuation means the probe’s output will be one-half of the actual settled voltage.

In theory, this circuit allows settling to be observed to small amplitudes. In practice, it cannot be relied upon to produce useful measurements. The oscilloscope connection presents problems. As probe capacitance rises, AC loading of the resistor junction influences observed settling waveforms. A 10pF probe alleviates this problem but its 10× attenuation sacrifices oscilloscope gain. 1× probes are not suitable because of their excessive input capacitance. An active

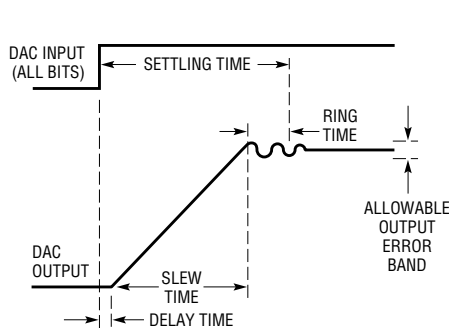


Figure 1. DAC-settling-time components include delay, slew and ring times. Fast amplifiers reduce slew time, although longer ring time usually results. Delay time is normally a small term.

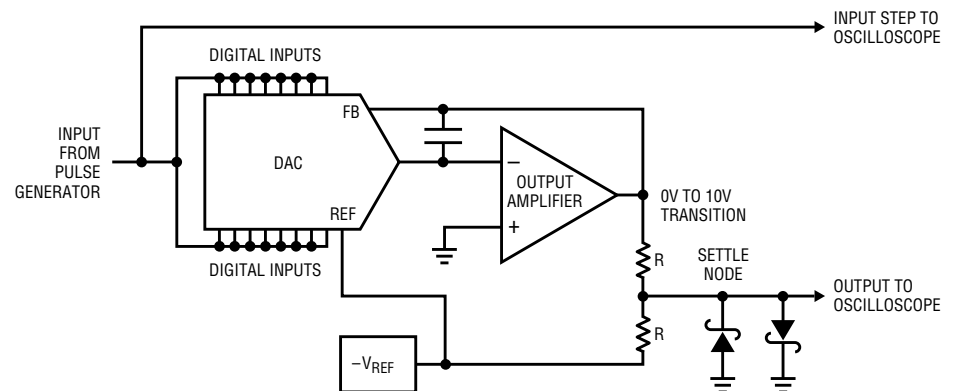


Figure 2. Popular summing scheme for DAC-settling-time measurement provides misleading results. 16-bit measurement causes >200× oscilloscope overdrive. Displayed information is meaningless.

Components for 16-Bit D/A Conversion

Components suitable for 16-bit D/A conversion are members of an elite class. 16 binary bits is one part in 65,536—just 0.0015% or 15 parts-per-million. This mandates a vanishingly small error budget and the demands on components are high. The digital-to-analog converters listed in Table A all use Si-Chrome thin-


film resistors for high stability and linearity over temperature. Gain drift is typically 1ppm/°C or about 2LSBs over 0°C to 70°C. The amplifiers shown contribute less than 1LSB error over 0°C to 70°C with 16-bit DAC driven settling times of 1.7μs available. The references offer drifts as low as 1LSB over 0°C to 70°C with initial trimmed accuracy to 0.05% 

Table A. Short-form descriptions of components suitable for 16-bit digital-to-analog conversion

Component Type	Error Contribution Over 0°C to 70°C	Comments
LTC1597 DAC	≈2LSB Gain Drift 1LSB Linearity	Full Parallel Inputs Current Outputs
LTC1595 DAC	≈2LSB Gain Drift 1LSB Linearity	Serial Input 8-Pin Package Current Output
LTC1650 DAC	≈3.5LSB Gain Drift 6LSB Offset 4LSB Linearity	Complete Voltage Output DAC
LT1001 Amplifier	<1LSB	Good Low Speed Choice 10mA Output Capability
LT1012 Amplifier	<1LSB	Good Low Speed Choice Low Power Consumption
LT1468 Amplifier	<2LSB	1.7μs Settling to 16 Bits Fastest Available
LM199A Reference: 6.95V	≈1LSB	Lowest Drift Reference in this Group
LT1021 Reference: 10V	≈4LSB	Good General Purpose Choice
LT1027 Reference: 5V	≈4LSB	Good General Purpose Choice
LT1236 Reference: 10V	≈10LSB	Trimmed to 0.05% Absolute Accuracy
LT1461 Reference: 4.096V	≈10LSB	Recommended for LTC1650 DACs (see Above)

1× FET probe will work, but another issue remains.

The clamp diodes at the settle node are intended to reduce swing during amplifier slewing, preventing excessive oscilloscope overdrive. Unfortunately, oscilloscope overdrive recovery characteristics vary widely among different types and are not usually specified. The Schottky diodes' 400mV drop means the oscilloscope may see an unacceptable overload, bringing displayed results into question.

At 10-bit resolution (10mV at the DAC output—5mV at the oscilloscope), the oscilloscope typically undergoes a 2× overdrive at 50mV/DIV and the desired 5mV baseline is just discernible. At 12-bit or higher resolution, the measurement becomes hopeless with this arrangement. Increasing oscilloscope gain brings commensurate increased vulnerability to overdrive induced errors. At 16 bits, there is clearly no chance of measurement integrity.

The preceding discussion indicates that measuring 16-bit settling time requires a high gain oscilloscope that is somehow immune to overdrive. The gain issue is addressable with an external wideband preamplifier that accurately amplifies the diode-clamped settle node. Getting around the overdrive problem is more difficult.

The only oscilloscope technology that offers inherent overdrive immunity is the classical sampling 'scope.

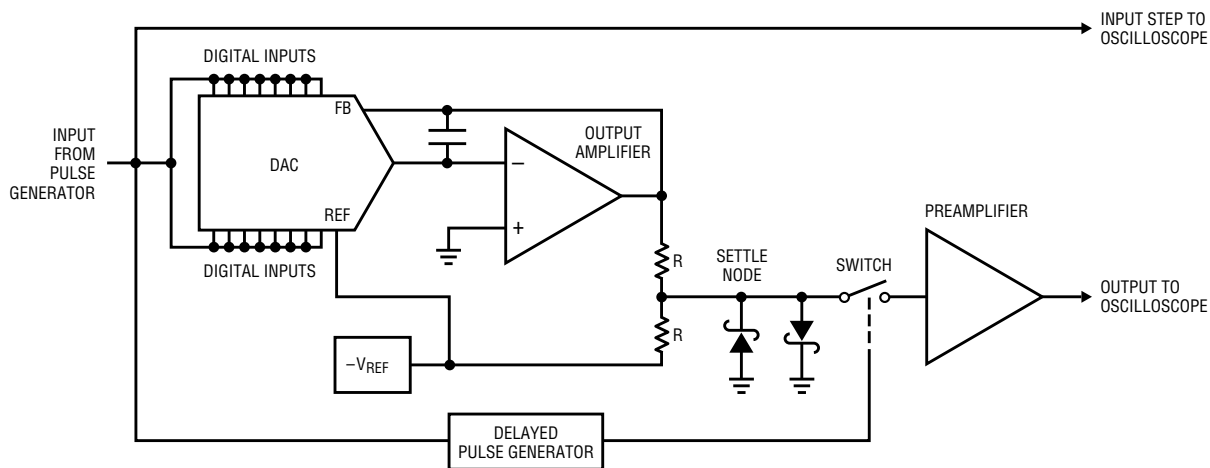


Figure 3. Conceptual arrangement eliminates oscilloscope overdrive. A delayed pulse generator controls the switch, preventing the oscilloscope from monitoring settle node until settling is nearly complete.

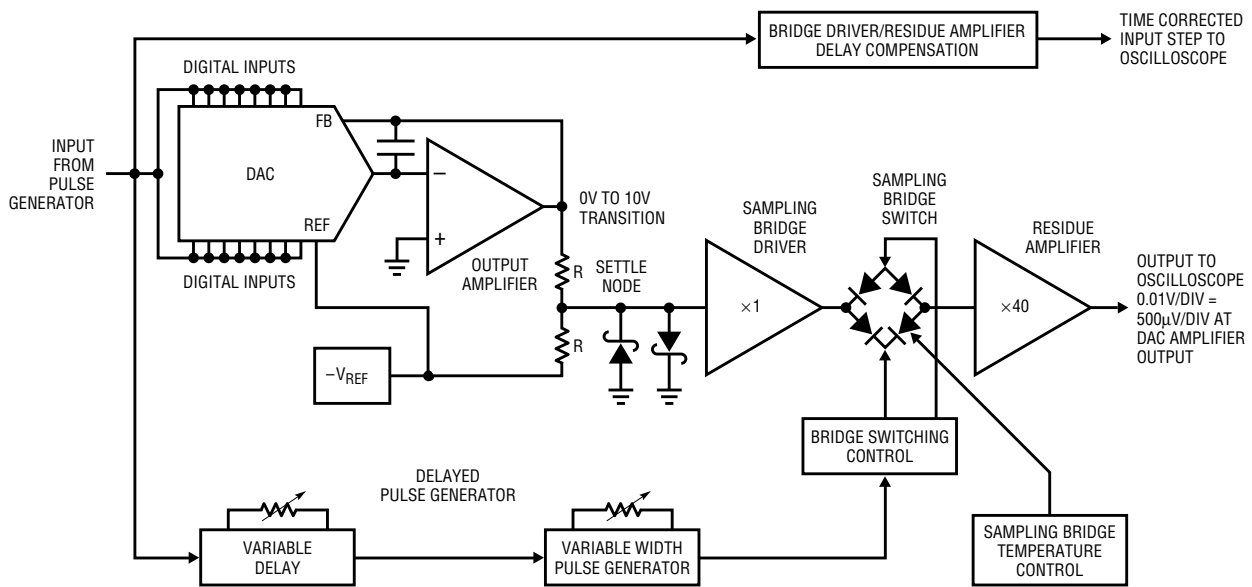


Figure 4. Block diagram of DAC-settling-time measurement scheme: diode bridge switch minimizes switching feedthrough, preventing residue-amplifier oscilloscope overdrive. Temperature control maintains 10µV switch offset baseline. Input step-time reference is compensated for ×1 and ×40 amplifier delays.

Unfortunately, these instruments are no longer manufactured (although still available on the secondary market). It is possible, however, to construct a circuit that borrows the overload advantages of classical sampling 'scope technology. Additionally, the circuit can be endowed with features particularly suited for measuring 16-bit DAC settling time.

Practical DAC-Settling-Time Measurement

Figure 3 is a conceptual diagram of a 16-bit DAC-settling-time measurement circuit. This figure shares attributes with Figure 2, although some new features appear. In this case, the preamplified oscilloscope is connected to the settle point by a switch. The switch state is determined by a delayed pulse generator, which is triggered from the same pulse that controls the DAC. The delayed pulse generator's timing is arranged so that the switch does not close until settling is very nearly complete. In this way the incoming waveform is sampled in time, as well as amplitude. The oscilloscope is never subjected to overdrive—no off-screen activity ever occurs.

Figure 4 is a more complete representation of the DAC settling time scheme. Figure 3's blocks appear in

greater detail and some new refinements show up. The DAC-amplifier summing area is unchanged. Figure 3's delayed pulse generator has been split into two blocks; a delay and a pulse generator, both independently variable. The input step to the oscilloscope runs through a section that compensates for the propagation delay of the settling-time-measurement path. The most striking new aspect of the diagram is the diode bridge switch. Borrowed from classical sampling oscilloscope circuitry, it is the key to the measurement. The diode bridge's inherent balance eliminates charge-

injection-based errors in the output. It is far superior to other electronic switches in this characteristic. Any other high speed switch technology contributes excessive output spikes due to charge-based feedthrough. FET switches are not suitable because their gate-channel capacitance permits such feedthrough. This capacitance allows gate-drive artifacts to corrupt the oscilloscope display, inducing overload and defeating the switch's purpose.

The diode bridge's balance, combined with matched, low capacitance, monolithic diodes and complementary high speed switching, yields a cleanly

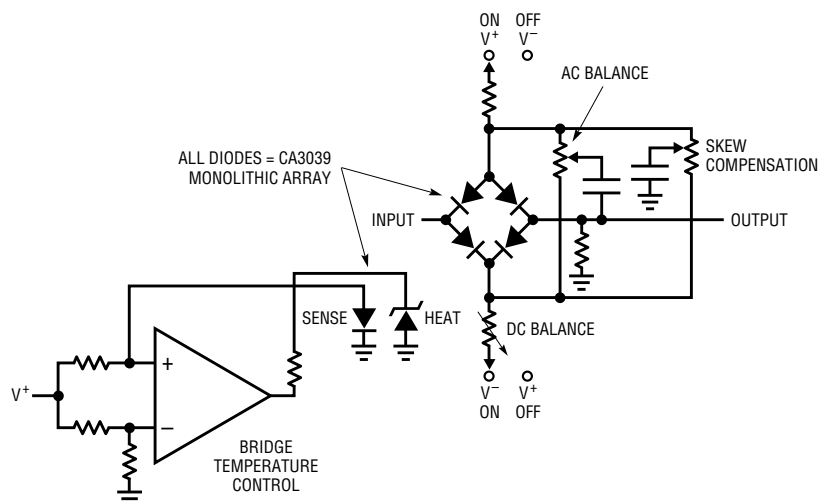


Figure 5. Diode bridge switch trims include AC and DC balance and switch drive timing skew. Remaining diodes in monolithic array are used for temperature control.

switched output. The monolithic diode bridge is also temperature controlled, providing a bridge offset error below 10 μ V, stabilizing the measurement baseline. The temperature control is implemented using uncommitted diodes in the monolithic array as heater and sensor.


Figure 5 details considerations for the diode bridge switch. The bridge diodes tend to cancel each other's temperature coefficient—unstabilized bridge drift is about 100 μ V/ $^{\circ}$ C and the temperature control reduces residual drift to a few microvolts/ $^{\circ}$ C.

Bridge temperature control is achieved by using one diode as a sensor. Another diode, running in reverse breakdown ($V_Z \approx 7V$), serves as the heater. The control amplifier, comparing the sensor diode to a voltage at its negative terminal, drives the heater diode to temperature stabilize the array.

DC balance is achieved by trimming the bridge on-current for zero input-output offset voltage. Two AC trims are required. The "AC balance" corrects for diode and layout capacitive imbalances and the "skew compensation" corrects for any timing asymmetry in the nomi-

nally complementary bridge drive. These AC trims compensate small dynamic imbalances that could result in parasitic bridge outputs.

Conclusion

This concludes part one of this article. Part two, which will appear in the November issue of *Linear Technology* magazine, details the settling time circuitry and presents results. Both parts represent a distillation of a full-length LTC application note, AN74, *Component and Measurement Advances Ensure 16-Bit DAC Settling Time*. 

New 16-Bit Bipolar Output DAC in Narrow SO-16 Package

by Hassan Malik


Linear Technology introduces its first bipolar, voltage output 16-bit digital to analog converter, the LTC1650. The LTC1650 is available in a narrow 16-pin SO package, making it the smallest bipolar, 16-bit voltage output DAC on the market today. The LTC1650 operates from $\pm 5V$ supplies and draws 5mA. It is equipped with a rail-to-rail, low noise, deglitched output amplifier that can be configured to operate in a unipolar or bipolar mode. The mid-scale glitch is under 2nV-s and the full-scale settling time in unipolar mode is 4 μ s.

The LTC1650 is 16-bit monotonic over the industrial temperature range,

with a typical differential nonlinearity of less than $\pm 0.3LSB$. Figures 1 and 2 show a typical application for the part and its DNL curve. The LTC1650 is equipped with an output-span-setting resistor tied to the UNI/BIP pin. When this pin is tied to the V_{OUT} pin, the output will swing from REFLO to REFHI; when the pin is tied to REFHI, the output swings from $-REFHI$ to REFHI.

The LTC1650 has a user-defined voltage to which its output resets on power-up or when the part is cleared. The voltage on the V_{RST} pin is applied to the output through a transmission gate when the part powers up or is

cleared. There are supply brown-out detectors on all three supplies, AV_{DD} , DV_{DD} and AV_{SS} . When any of these supplies drops below 2.5V, the part is cleared, connecting the output to V_{RST} , and the RSTOUT pin changes to a logic low.

The 3-wire serial interface of the LTC1650 is SPI/QSPI and MICRO-WIRETM compatible. All the logic inputs are TTL/CMOS compatible and the CLK input is equipped with a Schmitt trigger that allows direct optocoupler interfacing. There is also a D_{OUT} pin for daisy-chaining several DACs. The digital feedthrough is 0.05nV-s. 

MICROWIRE is a trademark of National Semiconductor Corp.

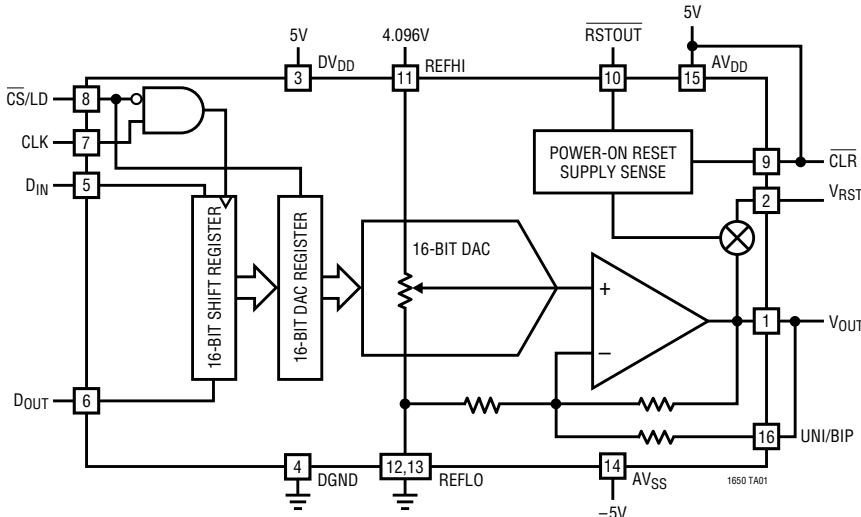


Figure 1. LTC1650 block diagram

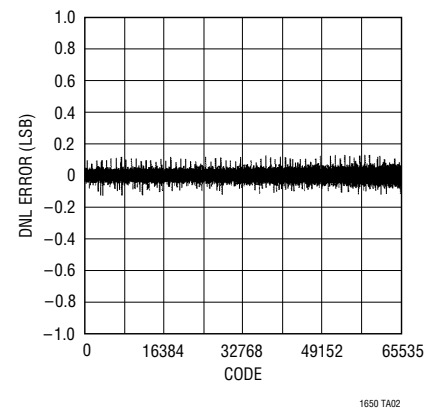


Figure 2. The LTC1650 bipolar output DAC has $\pm 0.3LSB$ typical DNL.


Low Noise 33V Varactor Bias Supply

by Jeff Witt

Wideband tuning circuits, such as those used in cable television systems, require a power supply for driving a varactor. This bias supply is usually at a voltage higher than the system supply voltage, allowing a large tuning range. The supply must have very little noise; voltage ripple, for example, can appear as sidebands on a local oscillator. This circuit takes

advantage of the fixed operating frequency of the LT1317B boost regulator to generate a low noise 33V bias voltage.

The circuit (Figure 1) is a simple boost regulator with its output voltage doubled by diodes D2 and D3 and capacitor C3. With this doubler, the circuit can generate an output voltage greater than the voltage rating of

the LT1317B's internal power switch. This supply can deliver 10mA at 33V from a 3V to 6V input, allowing operation from either 3.3V or 5V logic rails. The high operating frequency (600kHz) results in low, easily filtered output ripple, as shown in Figure 2. The high frequency also allows the use of small, low cost external components. 

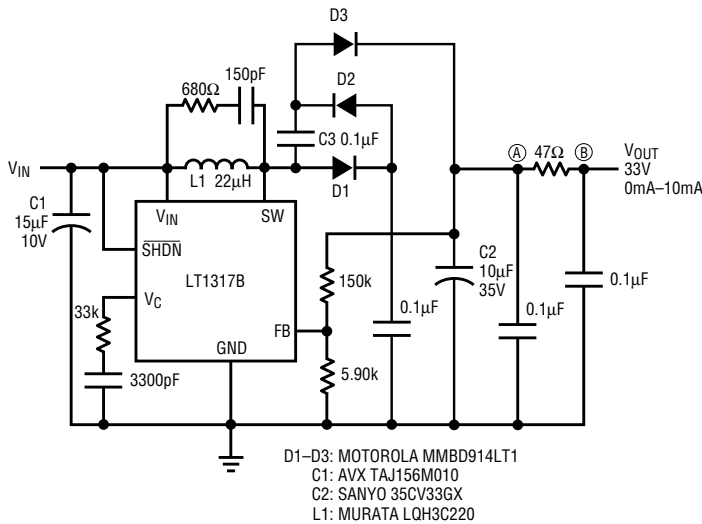


Figure 1. This circuit generates a low noise bias supply for varactor-based tuning circuits.

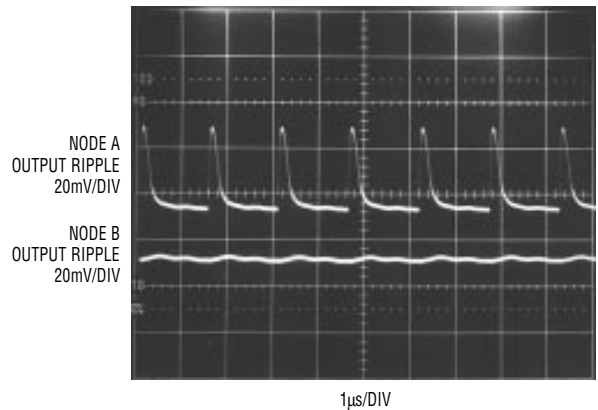


Figure 2. The output ripple of Figure 1's supply as it delivers 5mA at 33V from a 5V input; traces A and B show ripple before and after the RC output filter, respectively.

DESIGN IDEAS

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For further information on any of the devices mentioned in this issue of *Linear Technology*, use the reader service card or call the LTC literature service number:

1-800-4-LINEAR

Ask for the pertinent data sheets and Application Notes.

Low Noise LT1614 DC/DC Converter Delivers -5V at 200mA from 5V Input

by Steve Pietkiewicz

The inverting DC/DC converter function is traditionally realized with a capacitor-based charge pump. Although simple, the output impedances of the best charge pump solutions are in the 5Ω to 10Ω range, resulting in significant regulation issues when the load current increases beyond a few tens of milliamperes. The LT1614 inductor-based inverting DC/DC converter uses closed-loop regulation to obtain an output impedance of 0.1Ω, eliminating output voltage droop under load.

Figure 1 details the 5V to -5V converter circuit. The LT1614 contains an internal 0.6Ω switch rated at 30V,

allowing up to 28V differential between input and output. Quiescent current is 1mA and the device contains a low-battery detector with a 200mV reference voltage. The device switches at 600kHz, allowing the use of small, inexpensive external inductors and capacitors. In fact, the total cost of the components specified in Figure 1 (excluding the LT1614) is approximately \$0.70 in 10,000-piece quantities.

The LT1614 operates by driving its NFB pin to a voltage of -1.24V, allowing direct regulation of the negative output. This converter topology, which consists of inductors in series with

both input and output, results in low output noise and also in low reflected noise on the 5V input supply. The output and switch nodes are shown in Figure 2. Output ripple voltage of 40mV is due to the ESR of the tantalum output capacitor C2. Ripple voltage can be reduced substantially by replacing output capacitor C2 with a 10μF ceramic unit, as pictured in Figure 3.

In layout, be sure to tie D1's cathode directly to the LT1614's GND pin, as shown in Figure 1. This keeps the switching current loops tight and prevents the introduction of high frequency spikes on the output. The

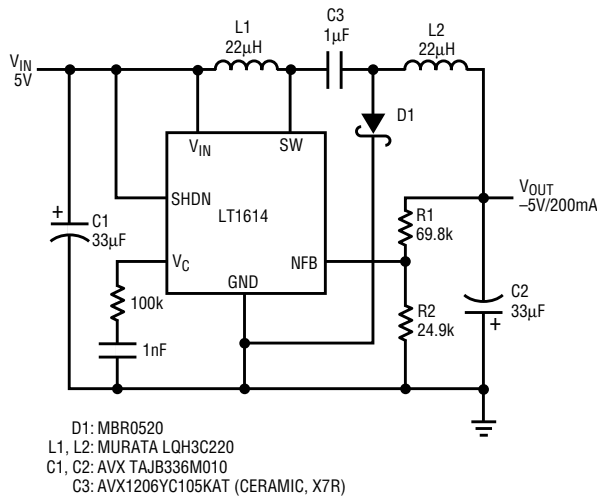


Figure 1. 5V to -5V DC/DC converter uses an inverting topology and delivers 200mA.

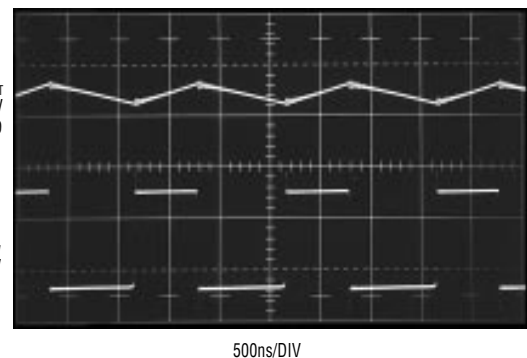


Figure 2. LT1614 output and switch node with a 33μF tantalum capacitor and 200mA load current

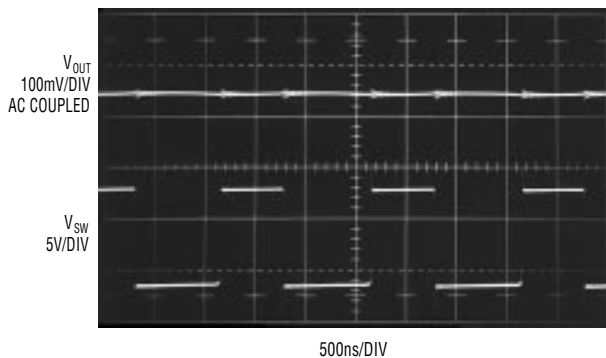


Figure 3. LT1614 output and switch node with a 10μF ceramic output capacitor and 200mA load current

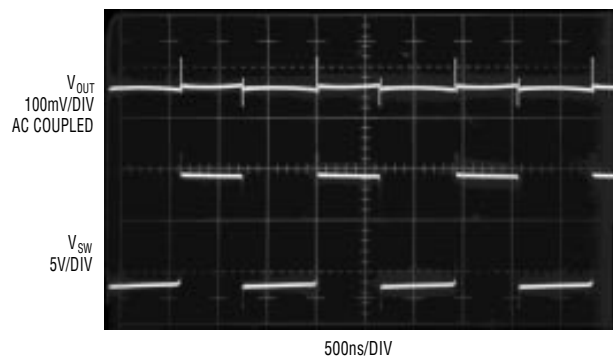



Figure 4. Improper placement of D1's cathode results in 60mV switching spikes at output, even with a 10μF ceramic output capacitor.

low noise that can be achieved with a ceramic capacitor may be corrupted by noise spikes if proper layout practice is not followed. To illustrate this point, output and switch waveforms from Figure 1's circuit, with a 10 μ F ceramic output capacitor and 200mA load, but with D1's cathode arbitrarily connected to the ground plane, are shown in Figure 4. 60mV switch-

ing spikes ruin an otherwise clean output.

Efficiency of the circuit is detailed in Figure 5. Efficiency reaches 73% at a 50mA load, and is above 70% at a 200mA load. Larger inductors with less copper resistance can be used to increase efficiency, although such inductors are more expensive than the Murata units specified. 

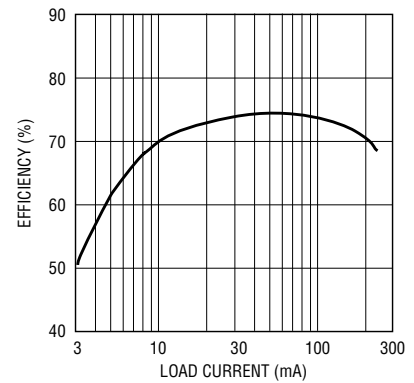


Figure 5. 5V to -5V converter efficiency reaches 73%.

4.5ns Dual-Comparator-Based Crystal Oscillator has 50% Duty Cycle and Complementary Outputs


by Joseph Petrofsky and Jim Williams

Figure 1's circuit uses the LT1720 dual comparator in a 50% duty cycle crystal oscillator. Output frequencies of up to 10MHz are practical.

Resistors at C1's positive input set a DC bias point. The 2k-0.068 μ F path furnishes phase-shifted feed-

back and C1 acts like a wideband, unity-gain follower at DC. The crystal's path provides resonant positive feedback and stable oscillation occurs. C2, sensing C1's input, provides a low skew, complementary output. A1 compares band-limited versions of

the outputs and biases C1's negative input. C1's only degree of freedom to respond is variation of pulse width; hence, the outputs are forced to 50% duty cycle.

The circuit operates with AT-cut fundamental crystals from 1MHz to 10MHz, over a 2.7V-6V power supply range. 50% duty cycle is maintained at all supply voltages, with output skew below 800 picoseconds. Figure 2 plots skew, which is seen to vary by about 800ps over a 2.7V-6V supply excursion. 

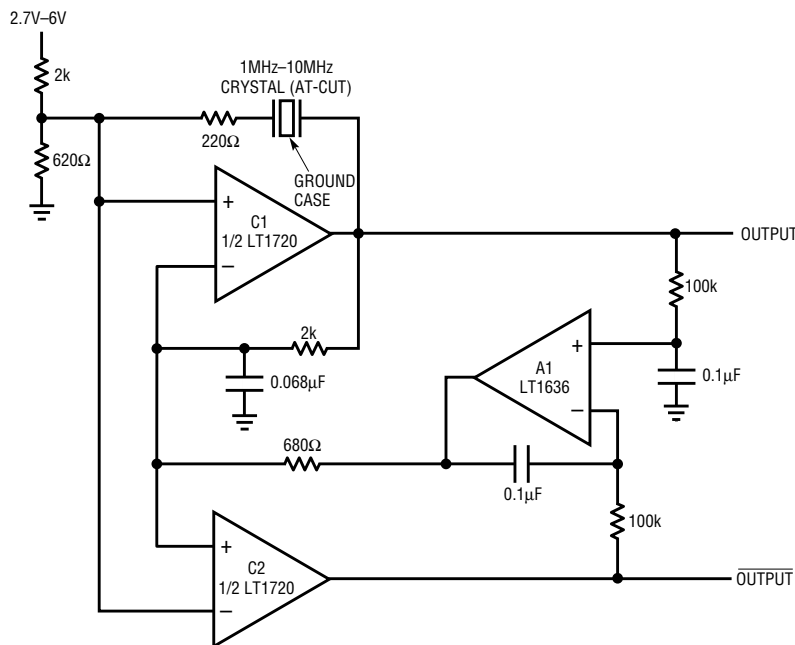


Figure 1. Crystal oscillator has complementary outputs and 50% duty cycle. A1's feedback maintains output duty cycle despite supply variations.

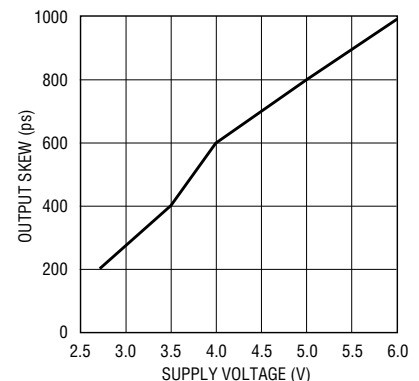


Figure 2. Output skew varies only 800ps over a 2.7V-6V supply excursion.

Battery Charger IC Doubles as Current Sensor


by Craig Varga

It's always fun to find applications for an IC that its designer never intended. The circuit shown in Figure 1 is such a design. In many cases, a circuit is required to provide a ground-referenced output voltage that is proportional to a measured current. Frequently, the current must be measured with a shunt in the positive rail that may be well above ground and, worse yet, may vary considerably with time. The LT1620 was originally intended as a controller for a synchronous buck regulator in battery-charger applications. The normal operating mode for this IC is to mirror a current signal down to a 5V reference supply. By adding a single small-signal MOSFET and a few resistors, it is pos-

sible to again mirror this signal to provide a ground referenced output.

Circuit operation is as follows: The LT1620 operates by producing a voltage between the V_{CC} pin and the AVG pin that is $10\times$ the voltage across sense resistor R5. C2 filters this voltage. An internal op amp has its noninverting input at the AVG pin (pin 8), its inverting input at the PROG pin (pin 7) and its output at the I_{OUT} pin (pin 2). With the circuit connected as shown in Figure 1, this amplifier will force enough current through R4 to make the voltage drop on R4 equal to the voltage across C2. This current is mirrored through R3 and is filtered by C3, producing a clean, ground-referenced, DC output voltage. Resistor R2 cancels a

small built-in offset in the LT1620's amplifiers. The output voltage obeys the following relationship: $V_O = I_L (R_5 \cdot R_3 \cdot 10) / R_4$. Changing the value of R3 selects different scale factors.

The circuit yields excellent linearity over a wide range of loads and input voltages. The curve shown in Figure 2 was measured with the sense resistor referenced to a 5V input source. The curve looks the same even at inputs over 25V, so only one curve is presented. Maximum input voltage is 36V. There is a small offset at no load, but in a typical microprocessor-based data acquisition system, only a simple 2-point calibration is needed to obtain absolute accuracy. 

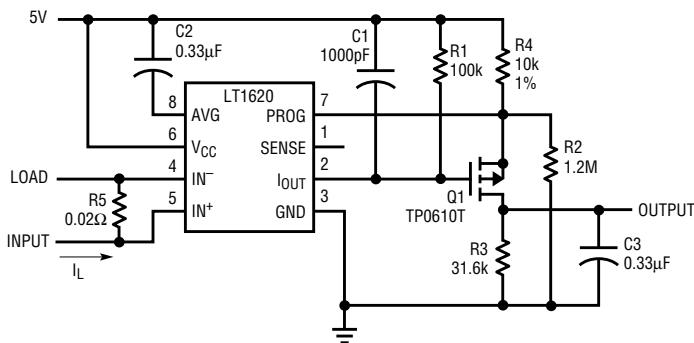


Figure 1. Current sensor schematic

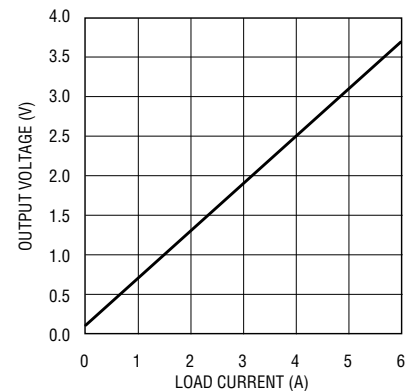


Figure 2. Transfer function

New Device Cameos

LT1671: A 60ns, 450µA, Single-Supply Comparator with Complementary Outputs and Output Latch

The LT1671 is a low power (450µA), fast (60ns), single-supply comparator designed to operate on either single 5V or $\pm 5V$ supplies. It has a maximum offset voltage of 2.5mV, complementary TTL compatible outputs and output-latch capability. The wide input-voltage range extends from the bottom supply rail to within 1.5V of

the top supply rail. The LT1671 is made with Linear Technology's new 6GHz complementary bipolar technology, which results in a dramatically improved speed/power product compared to industry-standard comparators developed in slower NPN-only technologies.

These features combine to make the LT1671 well suited for applications such as high performance crystal oscillators, single-supply voltage-to-frequency converters and high speed,

high accuracy level detectors. The LT1671 is offered in SO-8 and is pin compatible with the industry-standard LT1016 and LT1116 comparators.

The LTC1596-1: Ultra-Accurate, Low Power, 16-Bit Multiplying, Current-Output DAC Clears to Midscale

The latest addition to LTC's family of 16-bit current-output DACs is the multiplying LTC1596-1. Based on the LTC1596, this DAC features the same true 16-bit performance (DNL and INL, 1LSB maximum), the low glitch im-

pulse (1nV-s typical) and low supply current consumption (10 μ A maximum). The LTC1596-1 differs in its output magnitude after power is first applied or a reset is issued: whereas the LTC1596 resets to an output of zero, the LTC1596-1 resets to a midscale output.

Packaged in an SO-16 or 16-pin DIP, the LTC1596-1 operates on a single 5V supply. The DAC's reference input has an input range of $\pm 10V$. The LTC1596-1 can be configured for 2-quadrant or 4-quadrant multiplying applications. The device features a simple 3-wire serial interface and a D_{OUT} pin that allows daisy chaining.

LT1780/LT1781 RS232 Transceivers Meet IEC-1000-4-2 ESD Protection Standards

The popular LT1180A/LT1181A 2-driver, 2-receiver RS232 transceiver family has been expanded with new parts that pass the IEC-1000-4-2 level 4 ESD test. These new parts are designated the LT1780/LT1781. They are internally protected against $\pm 15kV$ air-gap or $\pm 8kV$ contact-mode discharges. The IEC-1000-4-2 test, formerly known as IEC-801-2, must be passed by all equipment sold in Europe. The on-chip protection of the LT1780/LT1781 eliminates the cost and board area required by external transient suppression devices that are usually required to successfully meet the IEC ESD protection requirements. The enhanced ESD protection has been achieved without compro-

missing the electrical performance of the device.

Present LT1180A/LT1181A users will see no change in electrical performance. The new 5V powered, 2-driver, 2-receiver device retains all of the electrical performance features that made the original part popular. Operation to 120kbaud with full 2500pF loads and up to 250kbaud with 1000pF loads is not degraded by the enhanced ESD protection devices.

The LT1780 is available in 18-pin DIP and SO packages. The LT1781 is available in 16-pin DIP and SO packages. The 18-pin versions include a Shutdown pin to conserve power and allow multiplexing of multiple transceivers.

LTC1143: SO-16 Dual, High Efficiency Switching Regulator Family Expands


Two new members of the LTC1143 dual, high efficiency step-down controller family, the LTC1143L and LTC1143L-ADJ, answer the need for lower input and output voltages in step-down DC/DC converters. The LTC1143L features a 3.5V to 14V operating voltage range (16V absolute maximum) with logic-controlled shutdown of fixed 3.3V and 5V channels, whereas the LTC1143L-ADJ combines the same input range with the versatility of two adjustable output voltage channels.

Already a very cost effective solution with two high efficiency switching regulator controllers in an SO-16 package, the LTC1143L extends operation

down to $V_{IN} = 3.5V$. As with the LTC1143, the two controllers feature fixed 3.3V and 5V outputs with individual shutdown pins. Extending operation to 3.5V allows the 3.3V channel to be used for standby power down to the end of life of 4-cell batteries with the 5V channel shut down.

The LTC1143L-ADJ provides cost effective surface mounted DC/DC conversion for reduced logic-supply voltages, such as 1.5V, 1.8V and 2.5V. It features two adjustable channels that allow the user to program the output voltages by using external resistive dividers. Although it gives up the logic-controlled shutdown pins to gain voltage adjustability, the LTC1143L-ADJ outputs can still be turned on and off for power supply sequencing purposes via a simple external network.

Device	V _{IN}	V _{OUT}
LTC1143	4V-16V	5V/3.3V Fixed
LTC1143L	3.5V-16V	5V/3.3V Fixed
LTC1143L-ADJ	3.5V-16V	Adj/Adj

The LTC1143 family controls external P-channel power MOSFETs using constant off-time current mode operation for excellent line and load regulation. All family members feature Burst Mode operation with only 160 μ A typical quiescent current per channel, programmable current limit and 100% duty cycle capability for ultralow dropout. They are available in a space saving small outline 16-pin plastic package. 



DESIGN TOOLS

Applications on Disk

FilterCAD™ 2.0 CD-ROM — This CD is a powerful filter design tool that supports all of Linear Technology's high performance switched capacitor filters. Included is filterView™, a document navigator that allows you to quickly find Linear Technology monolithic filter data sheets, the FilterCAD manual, application notes, design notes and *Linear Technology* magazine articles. It *does not* have to be installed to run FilterCAD. It is not necessary to use filterView to view the documents, as they are standard .PDF files, readable with any version of Adobe Acrobat™. FilterCAD runs on Windows® 3.1 or Windows 95. FilterView requires Windows 95. The FilterCAD program itself is also available on the web and will be included on the new LinearView™ CD.

Available at no charge.

Noise Disk — This IBM-PC (or compatible) program allows the user to calculate circuit noise using LTC op amps, determine the best LTC op amp for a low noise application, display the noise data for LTC op amps, calculate resistor noise and calculate noise using specs for any op amp.

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SPICE Macromodel Disk — This IBM-PC (or compatible) high density diskette contains the library of LTC op amp SPICE macromodels. The models can be used with any version of SPICE for general analog circuit simulations. The diskette also contains working circuit examples using the models and a demonstration copy of PSPICE™ by MicroSim.

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SwitcherCAD supports the following parts: LT1070 series: LT1070, LT1071, LT1072, LT1074 and LT1076. LT1082. LT1170 series: LT1170, LT1171, LT1172 and LT1176. It also supports: LT1268, LT1269 and LT1507. LT1270 series: LT1270 and LT1271. LT1371 series: LT1371, LT1372, LT1373, LT1375, LT1376 and LT1377.

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